Advanced LinCMOS Rail-to-Rail Operational Amplifiers

■ Description

The TLC2272 is dual operational amplifiers. The devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC2272 offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher-speed applications. These devices offer comparable AC performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC2272 has a noise voltage of 9 nV/√Hz, two times lower than competitive solutions.

The TLC2272 exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family is available with a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and±5 V.

■ Features

- Output Swing Includes Both Supply Rails
- Low Noise: 9 nV/√Hz Typical at f = 1 kHz
- Low-Input Bias Current: 1-pA Typical
- Fully-Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth: 2.2-MHz Typical
- High Slew Rate: 3.6-V/μs Typical
- Low Input Offset Voltage: 950 μV Maximum at T_A = 25°C
- Macromodel Included
- Available in Q-Temp Automotive

■ Applications

- White Goods (Refrigerators, Washing Machines)
- Hand-held Monitoring Systems
- Configuration Control and Print Support
- Transducer Interfaces
- Battery-Powered Applications

Maximum Peak-to-Peak Output Voltage vs Supply Voltage

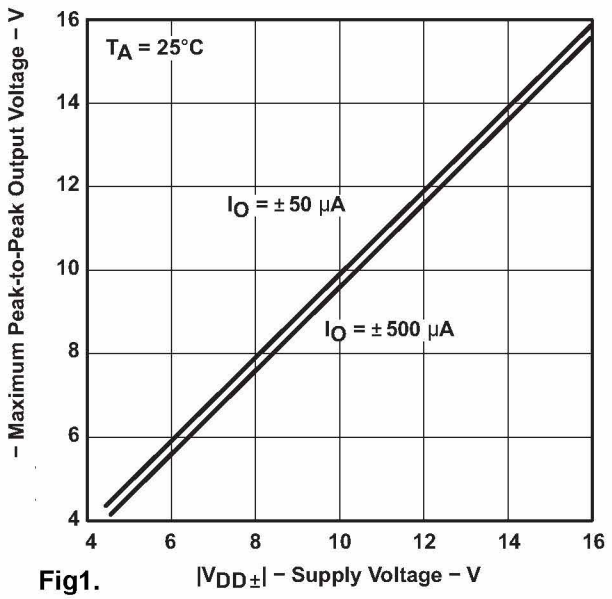


Fig1.

■ Ordering Information

Part Number	Package	Packing	Temperature(TA)	Package Qty	Remark
TLC2272CDR	SOIC-8	Reel	0°C~70°C	2500	
TLC2272IDR	SOIC-8	Reel	-40°C~125°C	2500	

■ Pin Assignment

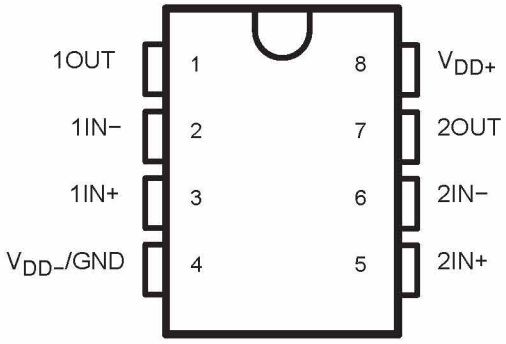


Fig2. SOIC-8 Package

■ Pin Description

NAME	PIN	I/O	DESCRIPTION
1IN+	3	I	Non-inverting input, Channel 1
1IN-	2	I	Inverting input, Channel 1
1OUT	1	O	Output, Channel 1
2IN+	5	I	Non-inverting input, Channel 2
2IN-	6	I	Inverting input, Channel 2
2OUT	7	O	Output, Channel 2
V_{DD+}	8	—	Positive (highest) supply
V_{DD-}/GND	4	—	Negative (lowest) supply

■ ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range(unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, $V_{DD}+$ (2)			8	V
$V_{DD}-$ (2)		–8		V
Differential input voltage, V_{ID} (3)			±16	V
Input voltage, V_I(any input) (2)		V_{DD-} – 0.3	V_{DD+}	V
Input current, I_I (any input)			±5	mA
Output current, I_O			±50	mA
Total current into V_{DD+}			±50	mA
Total current out of V_{DD-}			±50	mA
Duration of short-circuit current at (or below) 25°C (4)		Unlimited		
Operating free-air temperature range, T_A	C level parts	0	70	°C
	I, Q level parts	–40	125	
	M level parts	–55	125	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, P or PW package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package		300	°C
Storage temperature, T_{stg}		–65	150	°C

■ Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{DD±}$	Supply voltage	C LEVEL PARTS	±2.2	±8	V
		I LEVEL PARTS	±2.2	±8	
		Q LEVEL PARTS	±2.2	±8	
		M LEVEL PARTS	±2.2	±8	
V_I	Input voltage	C LEVEL PARTS	V_{DD-}	V_{DD+} –1.5	V
		I LEVEL PARTS	V_{DD-}	V_{DD+} –1.5	
		Q LEVEL PARTS	V_{DD-}	V_{DD+} –1.5	
		M LEVEL PARTS	V_{DD-}	V_{DD+} –1.5	
V_{IC}	Common-mode input voltage	C LEVEL PARTS	V_{DD-}	V_{DD+} –1.5	V
		I LEVEL PARTS	V_{DD-}	V_{DD+} –1.5	
		Q LEVEL PARTS	V_{DD-}	V_{DD+} –1.5	
		M LEVEL PARTS	V_{DD-}	V_{DD+} –1.5	
T_A	Operating free-air temperature	C LEVEL PARTS	0	70	°C
		I LEVEL PARTS	–40	125	
		Q LEVEL PARTS	–40	125	
		M LEVEL PARTS	–55	125	

■ ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	Q-grade and M-grade devices in D and PW packages	±2000	V
		Charged-device model (CDM), per AEC Q100-011	Q-grade and M-grade devices in D and PW packages	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

■ Electrical Characteristics V_{DD} = 5 V

At specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	TLC2272	T_A = 25°C		300	2500	μV
			TLC2272A			300	950	
			TLC2272	Full Range(1)			3000	
			TLC2272A				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				2		μV/°C
	Input offset voltage long-term drift(2)	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				0.002		μV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		0.5	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
I_{IB}	Input bias current	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		1	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\lvert V_{IO} \rvert \le$ 5 mV		T_A = 25°C	–0.3	2.5	4	V
				Full Range(1)	0	2.5	3.5	
V_{OH}	High-level output voltage	I_{OH} = –20 μA				4.99		V
		I_{OH} = –200 μA		T_A = 25°C	4.85	4.93		
				Full Range(1)	4.85			
		I_{OH} = –1 mA		T_A = 25°C	4.25	4.65		
				Full Range(1)	4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 μA			0.01		V
			I_{OL} = 500 μA	T_A = 25°C		0.09	0.15	
				Full Range(1)			0.15	
			I_{OL} = 5 mA	T_A = 25°C		0.9	1.5	
				Full Range(1)			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V; R_L = 10 kΩ(3)	C level part	T_A = 25°C	15	35		V/mV
				T_A = 0°C to 80°C	15			
			I level part	T_A = 25°C	15	35		
				T_A = –40°C to 85°C	15			
			Q level part	T_A = 25°C	10	35		
				T_A = –40°C to 125°C	10			
			M level part	T_A = 25°C	10	35		
				T_A = –55°C to 125°C	10			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V; R_L = 1 MΩ(3)				175		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		T_A = 25°C	70	75		dB
				Full Range(1)	70			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD} / 2, no load		T_A = 25°C	80	95		dB
				Full Range(1)	80			
I_{DD}	Supply currrent	V_O = 2.5 V, no load		T_A = 25°C		2.2	3	mA
				Full Range(1)			3	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ(3), C_L = 100 pF(3)		T_A = 25°C	2.3	3.6		V/μs
				Full Range(1)	1.7			

■ Electrical Characteristics V_{DD} = 5 V (continued)

At specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_n	Equivalent input noise voltage	f = 10 Hz			50		nV/√Hz
		f = 1 kHz			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			1		μV
		f = 0.1 Hz to 10 Hz			1.4		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ(3)	A_V = 1		0.0013%		
			A_V = 10		0.004%		
			A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ(3), C_L = 100 pF(3)			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ(3), C_L = 100 pF(3)			1		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ(3), Step = 0.5 V to 2.5 V, C_L = 100 pF(3)	To 0.1%		1.5		μs
			To 0.01%		2.6		
φ_m	Phase margin at unity gain	R_L = 10 kΩ(3), C_L = 100 pF(3)			50°		
	Gain margin	R_L = 10 kΩ(3), C_L = 100 pF(3)			10		dB

(3) Referenced to 0 V.

■ Electrical Characteristics $V_{DD±}$ = ±5 V

At specified free-air temperature, $V_{DD±}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	TLC2272	T_A = 25°C		300	2500	μV
			TLC2272A			300	950	
			TLC2272	Full Range(1)			3000	
			TLC2272A				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				2		μV/°C
	Input offset voltage long-term drift(2)	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				0.002		μV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		0.5	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
I_{IB}	Input bias current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		1	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\lvert V_{IO} \rvert \le$ 5 mV		T_A = 25°C	–5.3	0	4	V
				Full Range(1)	–5	0	3.5	
V_{OM+}	Maximum positive peak output voltage	I_O = –20 μA				4.99		V
		I_O = –200 μA		T_A = 25°C	4.85	4.93		
				Full Range(1)	4.85			
		I_O = –1 mA		T_A = 25°C	4.25	4.65		
				Full Range(1)	4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 μA			–4.99		V
			I_O = 500 μA	T_A = 25°C	–4.85	–4.91		
				Full Range(1)	–4.85			
			I_O = 5 mA	T_A = 25°C	–3.5	–4.1		
				Full Range(1)	–3.5			

(1) T_A = –55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to TA = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

■ Electrical Characteristics $V_{DD±}$ = ±5 V (continued)

At specified free-air temperature, $V_{DD±}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V; R_L = 10 kΩ	C level part	T_A = 25°C	25	50		V/mV
				T_A = 0°C to 80°C	25			
			I level part	T_A = 25°C	25	50		
				T_A = –40°C to 85°C	25			
			Q level part	T_A = 25°C	20	50		
				T_A = –40°C to 125°C	20			
			M level part	T_A = 25°C	20	50		
				T_A = –55°C to 125°C	20			
		V_O = ±4 V; R_L = 1 MΩ				300		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = –5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C	75	80		dB
				Full Range[1]	75			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD+} = 2.2 V to ±8 V, V_{IC} = 0 V, no load		T_A = 25°C	80	95		dB
				Full Range[1]	80			
I_{DD}	Supply currrent	V_O = 0 V, no load		T_A = 25°C		2.4	3	mA
				Full Range[1]			3	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF		T_A = 25°C	2.3	3.6		V/μs
				Full Range[1]	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		μV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = ±2.3, f = 20 kHz, R_L = 10 kΩ		A_V = 1		0.0011%		
				A_V = 10		0.004%		
				A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF				2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF				0.54		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ, Step = –2.3 V to 2.3 V, C_L = 100 pF		To 0.1%		1.5		μs
				To 0.01%		3.2		
$φ_m$	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF				52°		
	Gain margin	R_L = 10 kΩ, C_L = 100 pF				10		dB

■ Functional Block Diagram

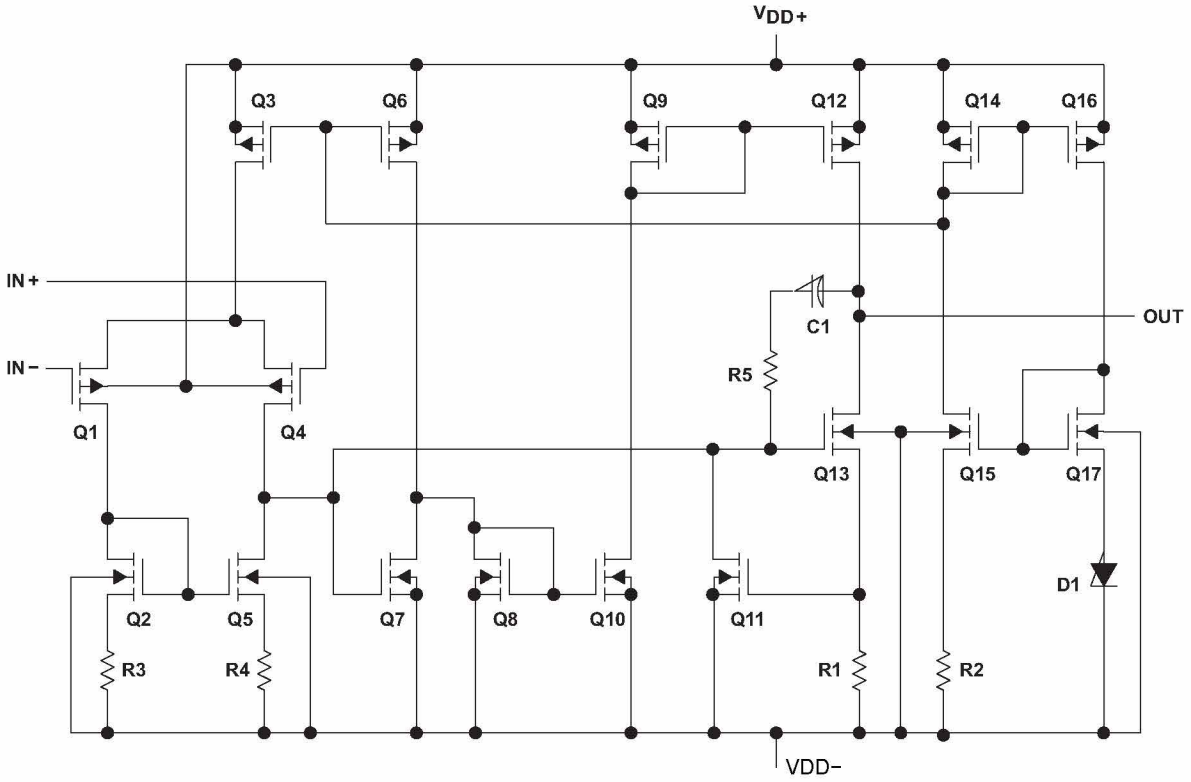


Fig3. Functional Block Diagram

Device Component Count(1)

Component	TLC2272
Transistors	38
Resistors	26
Diodes	9
Capacitors	3

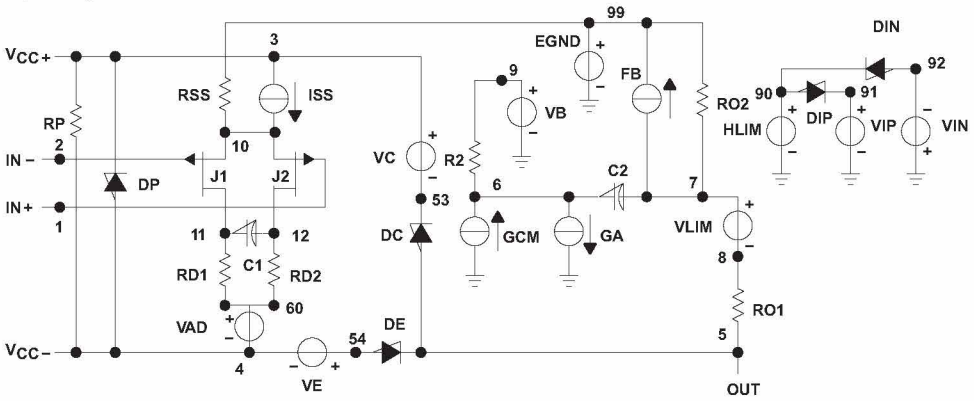
(1) Includes both amplifiers and all ESD, bias, and trim circuitry.

■ Application Information

Macromodel Information

Macromodel information provided was derived using MicroSim Parts™, the model generation software used with MicroSim PSpice™. The Boyle macromodel (1) and subcircuit in Fig 4 were generated using the TLC227x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- DC output resistance
- AC output resistance
- Short-circuit output current limit
- Common-mode rejection ratio
- Phase margin




```
.SUBCKT TLC227x 1 2 3 4 5
C1      11      12      1214E-12
C2      6       7       760.00E-12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,) 0 .5 .5
FB      99      0       POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 -1E6 1E6 1E6 -1E6
GA      6       0       11 12 377.0E-6
GCM 0 6 10 99 134E-9
ISS     3       10      DC 216.OE-6
HLIM    90      0       VLIM 1K
J1      11      1       210 JX
J2      12      1       110 JX
R2      6       9       100.OE3
RD1     60      11      2.653E3
RD2     60      12      2.653E3
R01     8       5       50
R02     7       9       50
RP      3       4       4.310E3
RSS     10      99      925.9E3
VAD     60      4       -.5
VB      9       0       DC 0
VC 3 53 DC .78
VE      54      5       DC .78
VLIM    7       8       DC 0
VLP     91      0       DC 1.9
VLN     0       92      DC 9.4
.MODEL DX D (IS=800.0E-18)
.MODEL JX PJF (IS=1.500E-12BETA=1.316E-3
+ VTO=-.270)
.ENDS
```

Fig 4. Boyle Macromodel and Subcircuit

(1) *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

■ Typical Application

High-Side Current Monitor

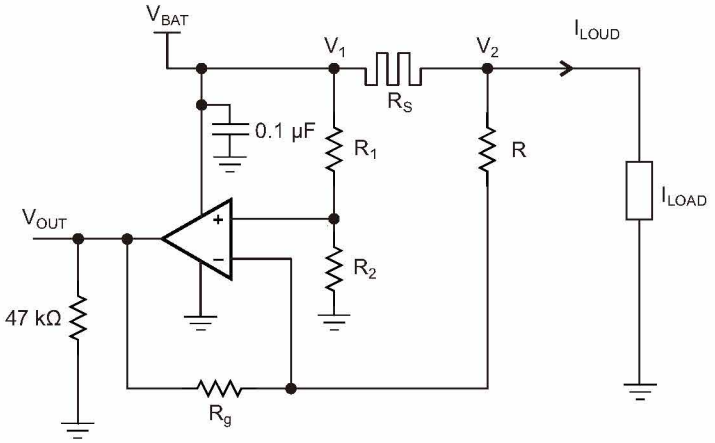


Fig 5. Equivalent Schematic (Each Amplifier)

Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

Differential Amplifier Equations

Equation 1 and Equation 2 are used to calculate V_{OUT}.

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1+\frac{R_1}{R_2}} \times \frac{V_1 + V_2}{2} + \frac{1+\frac{1}{2}\left(\frac{R_1}{R_2} + \frac{R}{R_g}\right)}{1+\frac{R_1}{R_2}}(V_1 - V_2)\right) \quad (1)$$

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1+\frac{R_1}{R_2}} \times V_{BAT} + \frac{1+\frac{1}{2}\left(\frac{R_1}{R_2} + \frac{R}{R_g}\right)}{1+\frac{R_1}{R_2}} \times R_S \times I_{Load}\right) \quad (2)$$

In an ideal case $R_1 = R$ and $R_2 = R_g$, and V_{OUT} can then be calculated using Equation 3:

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{Load} \quad (3)$$

However, as the resistors have tolerances, they cannot be perfectly matched.

$R_1 = R \pm \Delta R_1$
$R_2 = R_2 \pm \Delta R_2$
$R = R \pm \Delta R$
$R_g = R_g \pm \Delta R_g$

$$Tol = \frac{DR}{R} \quad (4)$$

By developing the equations and neglecting the second order, the worst case is when the tolerances add up. This is shown by Equation 5.

$$V_{OUT} = \pm (4\ Tol)\frac{R_g}{R+R_g} \times V_{BAT} + \left(1 \pm 2\ Tol\left(1+\frac{2R}{R+R_g}\right)\right)\frac{R_g}{R} \times R_S \times I_{LOAD}$$

where

- Tol = 0.01 for 1%
- Tol = 0.001 for 0.1%

(5)

If the resistors are perfectly matched, then Tol = 0 and V_{OUT} is calculated using Equation 6.

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{LOAD} \quad (6)$$

The highest error is from the Common mode, as shown in Equation 7.

$$4\ (Tol)\frac{R_g}{R+R_g} \times V_{BAT} \quad (7)$$

Gain of 10, $R_g / R = 10$, and Tol = 1%:

Common mode error = ((4 × 0.01) / 1.1) × 12 V = 0.436 V

Gain of 10 and Tol = 0.1%:

Common mode error = 43.6 mV

The resistors were chosen from 2% batches.

R_1 and R 12 kΩ
R_2 and R_g 120 kΩ

Ideal Gain = 120 / 12 = 10

The measured value of the resistors:

R_1 = 11.835 kΩ
R = 11.85 kΩ
R_2 = 117.92 kΩ
R_g = 118.07 kΩ

Application Curves

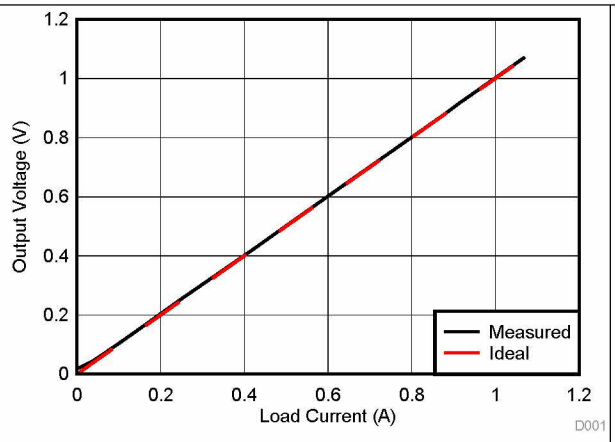


Fig 6. Output Voltage Measured vs Ideal (0 to 1 A)

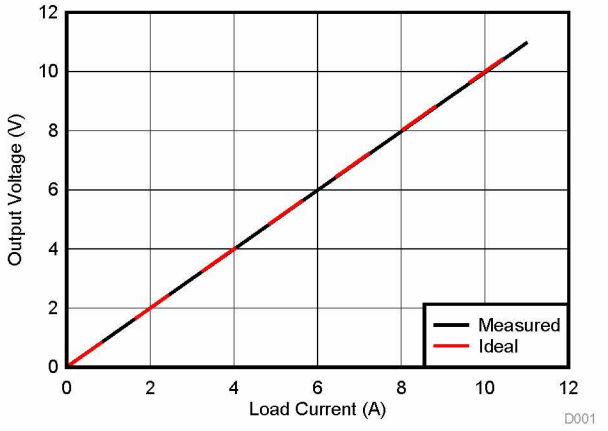


Fig 7. Output Voltage Measured vs Ideal (0 to 10 A)

■ Power Supply Recommendations

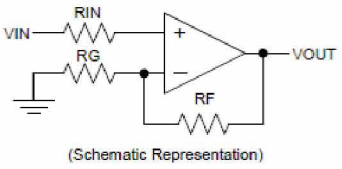
Supply voltage for a single supply is from 4.4 V to 16 V, and from ±2.2 V to ±8 V for dual supply. In the high-side sensing application, the supply is connected to a 12-V battery.

■ Layout

Layout Guidelines

The TLC227x and TLC227xA families of devices are wideband amplifiers. To realize the full operational performance of the devices, good high-frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1-μF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

Layout Example



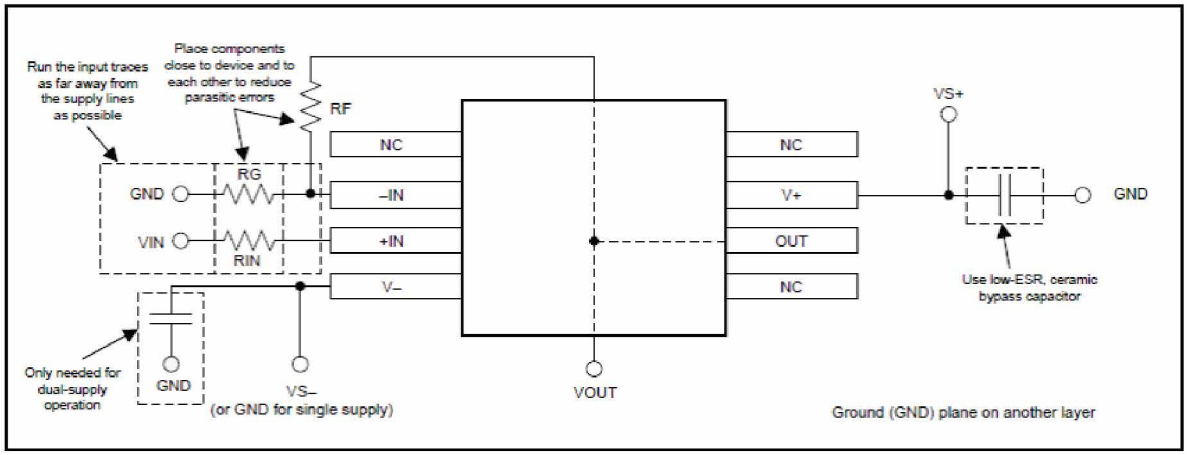
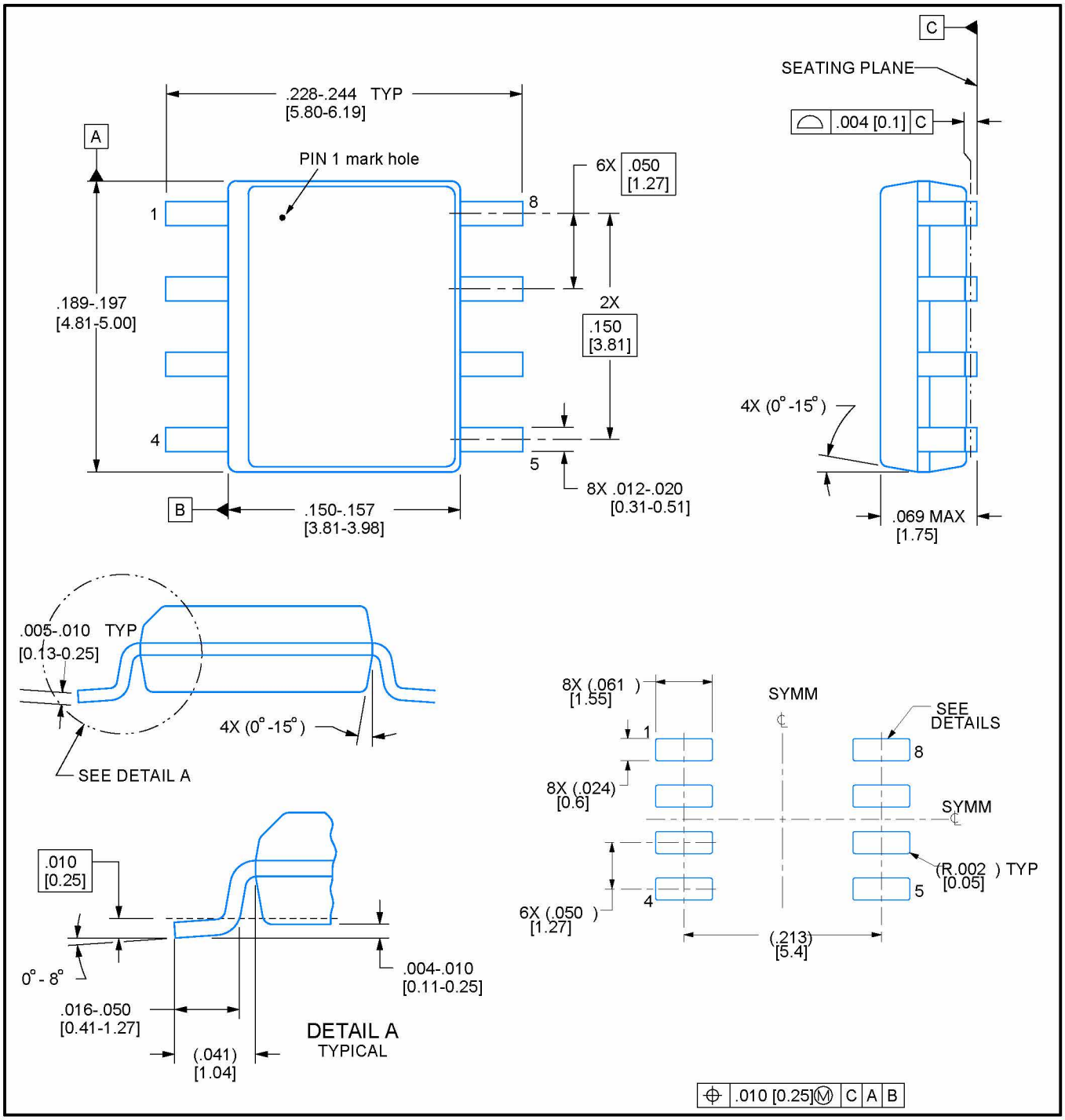


Fig 8. Layout Example

PACKAGE OUTLINE SOIC - 8,1.75 mm max height



NOTES: Linear dimensions are in inches [millimeters]. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.