LOW NOISE DUAL J-FET OPERATIONAL AMPLIFIER

■ Description

The TTESEMI TL072 is a high speed J-FET input dual operational amplifier. It incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit. The device features high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

■ Features

* Low input bias and offset current
* Wide common-mode (up to V_{CC}^{+}) and differential voltage range
* Output short-circuit protection
* High input impedance J-FET input stage
* Internal frequency compensation
* Latch up free operation
* High slewrate:10V/μs (typ.)
* Low noise en = 15nV /$\sqrt{Hz}$ (typ.)

■ Applications

- Solar energy: string and central inverter
- Motor drives: AC and servo drive control and power stage modules
- Single phase online UPS
- Three phase UPS
- Pro audio mixers
- Battery test equipment

■ Ordering Information

Part Number	Package	Packing	Temperature(TA)	Package Qty	Remark
TLC072CDR	SOIC-8	Reel	0°C~70°C	2500	
TLC072IDR	SOIC-8	Reel	-40°C~85°C	2500	

■ Pin Assignment

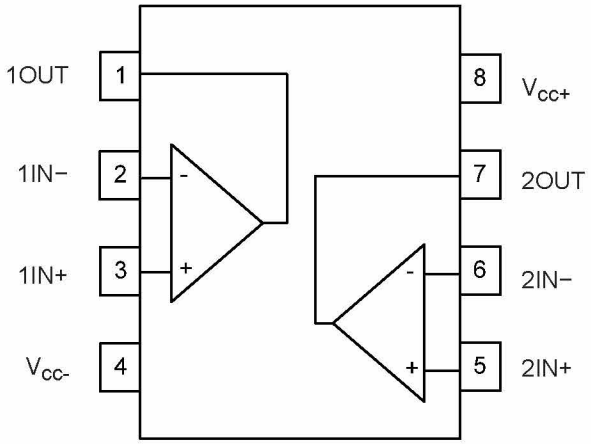


Fig1. SOIC-8 Package

■ Pin Description

NAME	PIN	I/O	DESCRIPTION
1IN+	3	I	Non-inverting input, Channel 1
1IN-	2	I	Inverting input, Channel 1
1OUT	1	O	Output, Channel 1
2IN+	5	I	Non-inverting input, Channel 2
2IN-	6	I	Inverting input, Channel 2
2OUT	7	O	Output, Channel 2
V_{cc+}	8	—	Positive (highest) supply
V_{cc-}	4	—	Negative (lowest) supply

■ ABSOLUTE MAXIMUM RATINGS

(TA=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage (Note 2)		V_{CC}	±18	V
Input Voltage (Note 3)		V_{IN}	±15	V
Differential Input Voltage (Note 4)		V_{ID}	±30	V
Power Dissipation	SOP-8	P_D	440	mW
Output Short-Circuit Duration (Note 5)			Infinite	
Operating Temperature		T_{OPR}	-40 ~ +125 (Note 6)	°C
Storage Temperature Range		T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}- and V_{CC}+.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
5. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
6. It is guarantee by design, not 100% be tested.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	125	°C/W
Junction to Case	SOP-8	θ_{JC}	40	°C/W

■ Electrical Characteristics

(VCC=±15V, TA=25 C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage (R_S=50Ω)	I_O	T_A=25°C		3	10	mV
		$T_{MIN} \le T_A \le T_{MAX}$			13	
Input Offset Voltage Drift	D_{VIO}			10		μV/°C
Input Offset Current (Note)	I_{IO}	T_A=25°C		5	100	pA
		$T_{MIN} \le T_A \le T_{MAX}$			10	nA
Input Bias Current (Note)	I_{IB}	T_A=25°C		20	200	pA
		$T_{MIN} \le T_A \le T_{MAX}$			20	nA
Input Common Mode Voltage Range	V_{ICM}		±11	-12~+15		V
Output Voltage Swing	$V_{O(SW)}$	T_A=25°C, R_L=2kΩ,	±1	±12		V
		T_A=25°C, R_L=10kΩ	±12	±13.5		V
		$T_{MIN} \le T_A \le T_{MAX}$, R_L=2kΩ	±10			V
		$T_{MIN} \le T_A \le T_{MAX}$, R_L=10kΩ	±12			V
Large Signal Voltage Gain (R_L=2kΩ, V_{OUT}=±10V)	Avd	T_A=25°C		200		V/mV
		$T_{MIN} \le T_A \le T_{MAX}$	15			
Gain Bandwidth Product (T_A=25°C)	GBP	V_{IN}=10mV, R_L=2kΩ, C_L=100pF, f=100kHZ	2.5	4		MHz
Input Resistance	R_I			10^{12}		Ω
Common Mode Rejection Ratio (R_S=50Ω)	CMR	T_A=25°C		86		dB
		$T_{MIN} \le T_A \le T_{MAX}$	70			
Supply Voltage Rejection Ratio (R_S=50Ω)	SVR	T_A=25°C		86		dB
		$T_{MIN} \le T_A \le T_{MAX}$	70			
Supply Current, No Load	I_{CC}	T_A=25°C		1.4	2.5	mA
Channel Separation (Av=100, T_A=25°C)	V_{01}/V_{02}			120		dB
Output Short-Circuit Current	I_{OS}	T_A=25°C	10	40	60	mA
		$T_{MIN} \le T_A \le T_{MAX}$	10		60	mA
Slew Rate (T_A=25°C)	SR	V_{IN}=10V, R_L=2kΩ C_L=100pF, unity gain	6	10		V/μs
Rise Time (T_A=25°C)	t_R	V_{IN} =20mV, R_L=2kΩ C_L=100pF, unity gain		0.1		μs
Overshoot (T_A=25°C)	K_{OV}	V_{IN}=20mV, R_L=2kΩ C_L=100pF, unity gain		10		%
Total Harmonic Distortion (T_A=25°C)	THD	A_V=20dB, f=1kHz, R_L=2kΩ, C_L=100pF, V_{OUT}=2Vpp)		0.01		%
Phase Margin	Φm			45		Degrees
Equivalent Input Noise Voltage (R_S=100Ω, f=1KHz)	eN			15		$\frac{nV}{\sqrt{Hz}}$

Note: The Input bias currents are junction leakage currents, which approximately double for every 10°C increase in the junction temperature.

■ PARAMETER MEASUREMENT INFORMATION

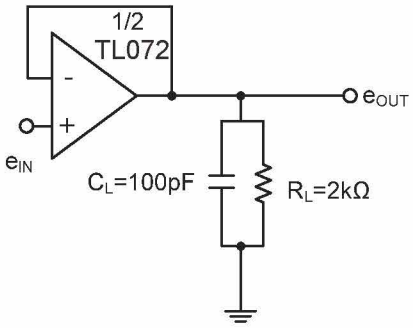


Fig2. Voltage Follower

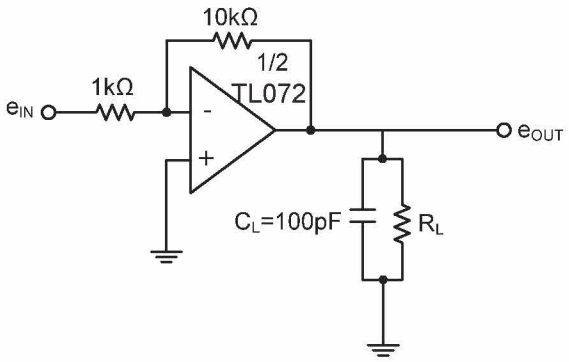


Fig3. Gain-of-10 Inverting Amplifier

■ Functional Block Diagram

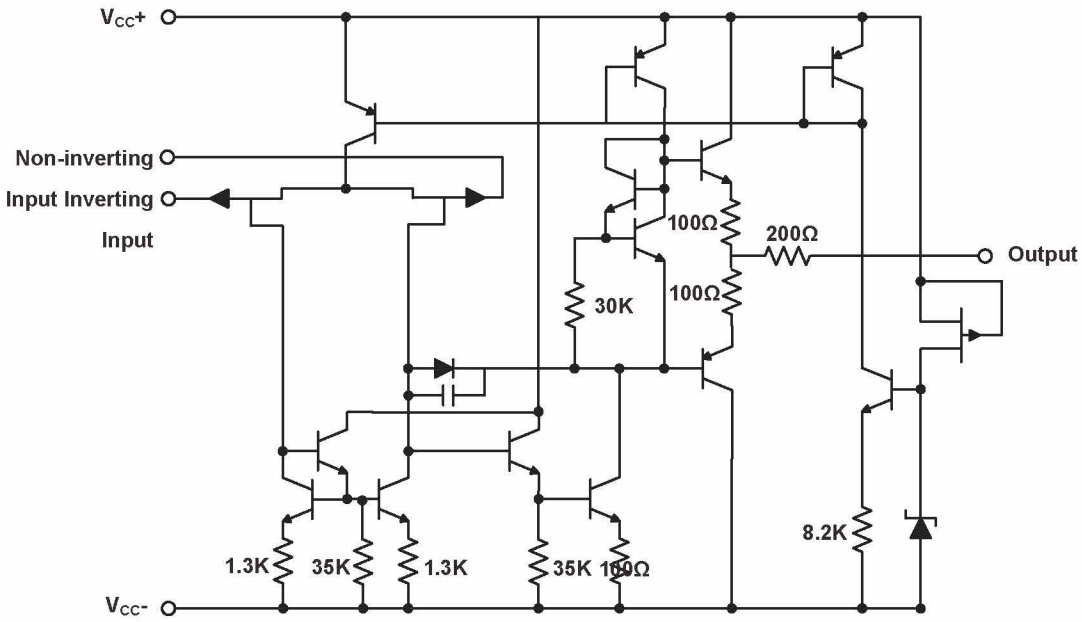
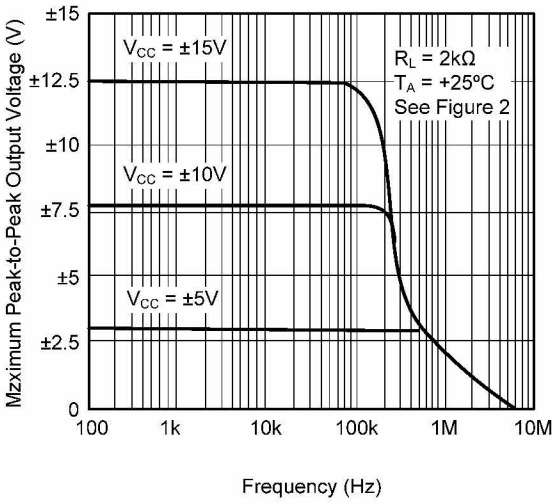


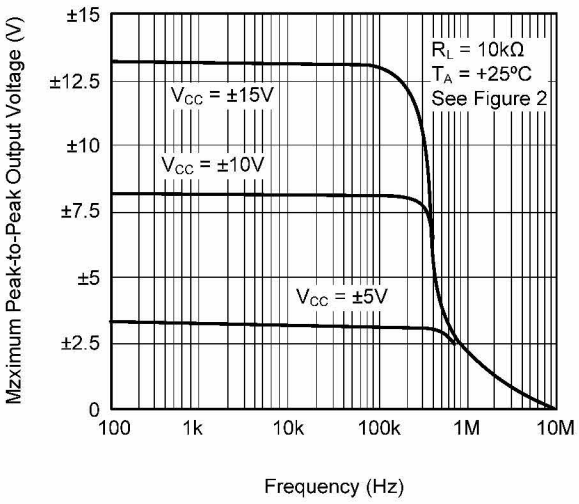
Fig4. Functional Block Diagram

■ TYPICAL CHARACTERISTICS

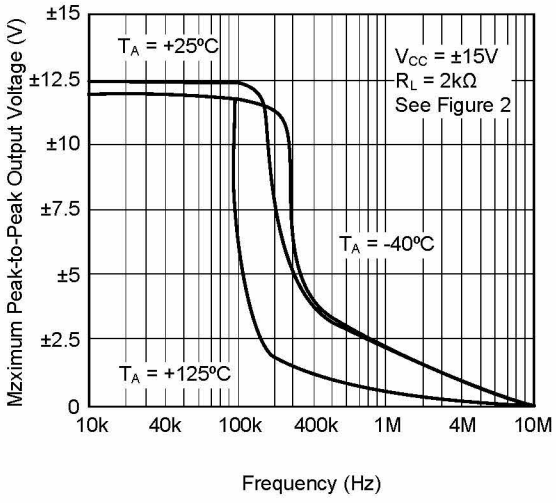
Maximum Peak-to-Peak Output Voltage vs. Frequency



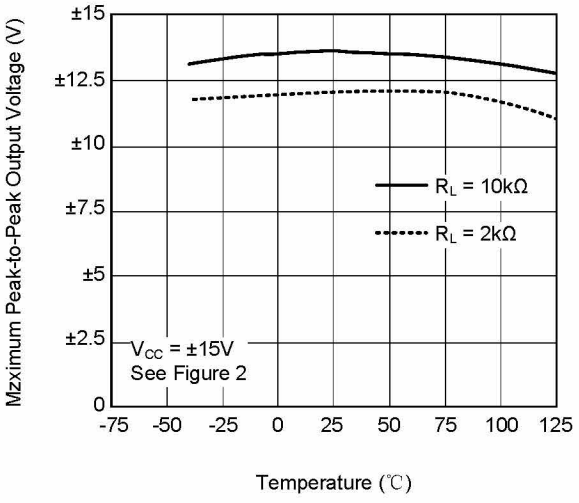
Maximum Peak-to-Peak Output Voltage vs. Frequency



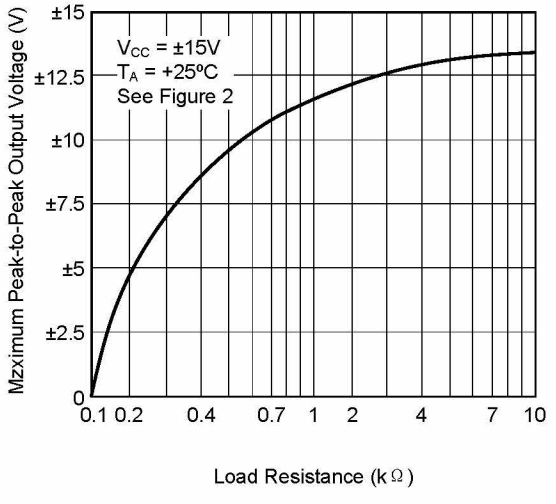
Maximum Peak-to-Peak Output Voltage vs. Frequency



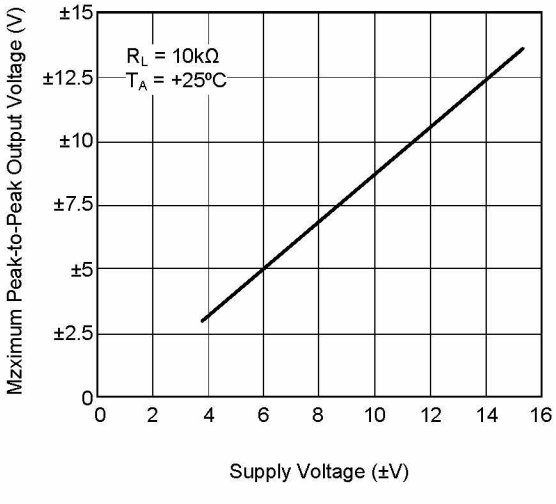
Maximum Peak-to-Peak Output Voltage vs. Free Air Temp.



Maximum Peak-to-Peak Output Voltage vs. Load Resistance

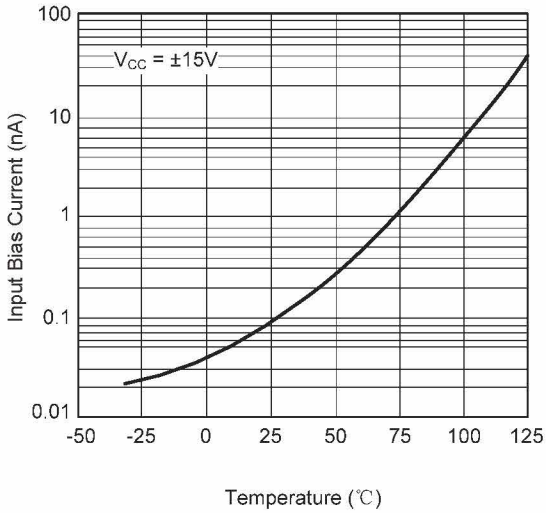


Maximum Peak-to-Peak Output Voltage vs. Supply Voltage

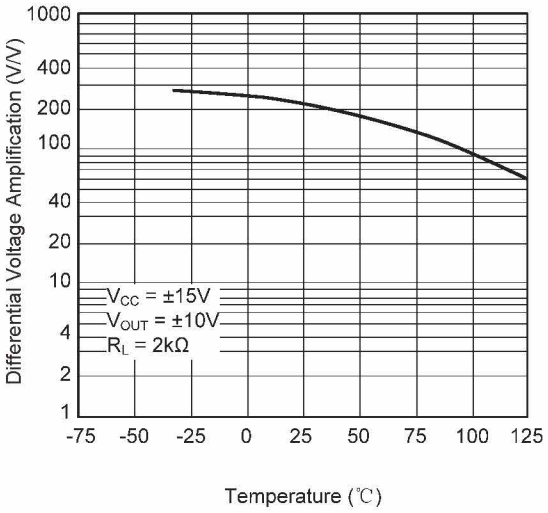


■ TYPICAL CHARACTERISTICS (Cont.)

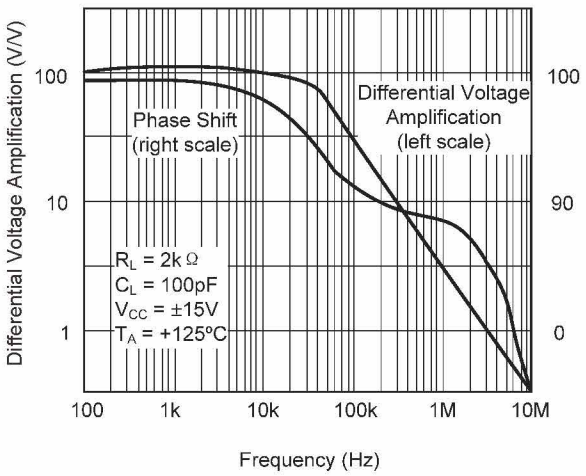
Input Bias Current vs. Free Air Temperature



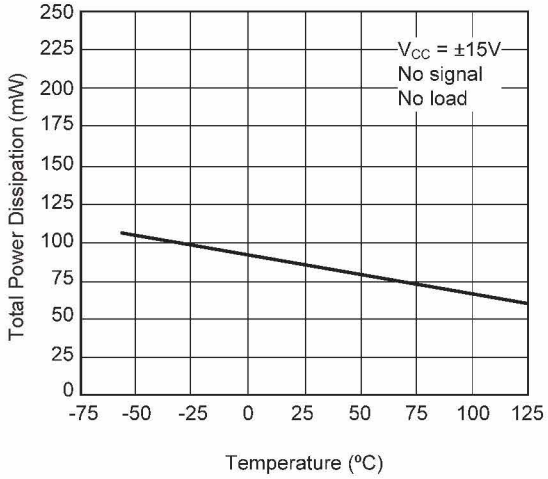
Large Signal Differential Voltage Amplification vs. Free Air Temperature



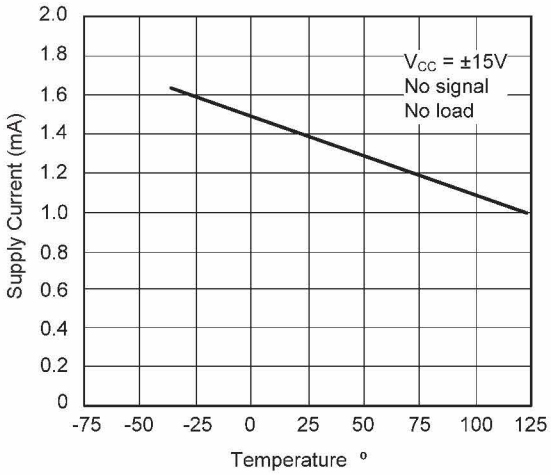
Large Signal Differential Voltage Amplification and Phase Shift vs. Frequency



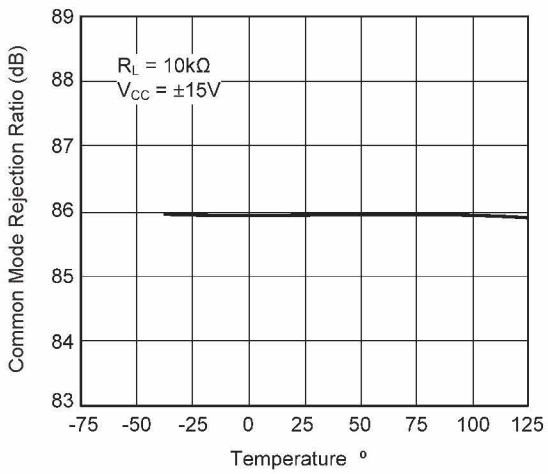
Total Power Dissipation vs. Free Air Temperature



Supply Current Per Amplifier vs. Free Air Temperature

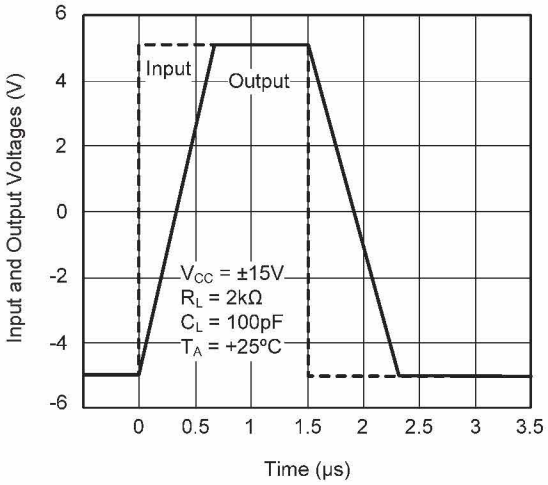


Total Power Dissipation vs. Free Air Temperature

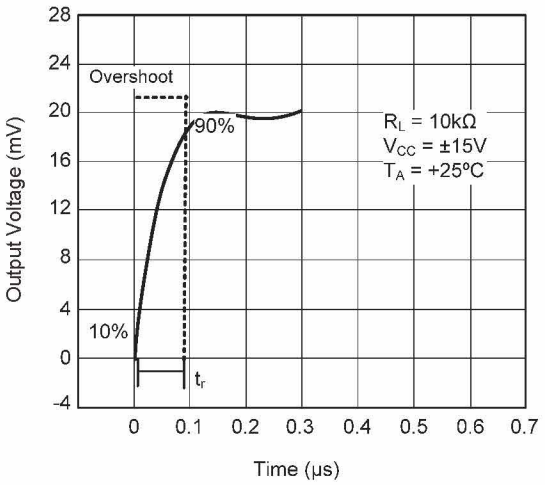


■ TYPICAL CHARACTERISTICS (Cont.)

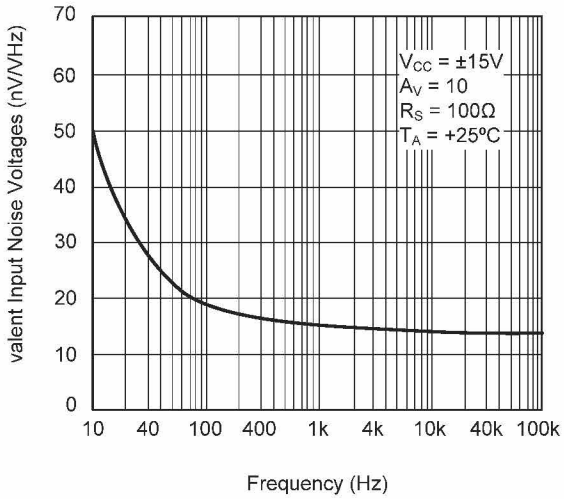
Voltage Follower Large Signal Pulse Response



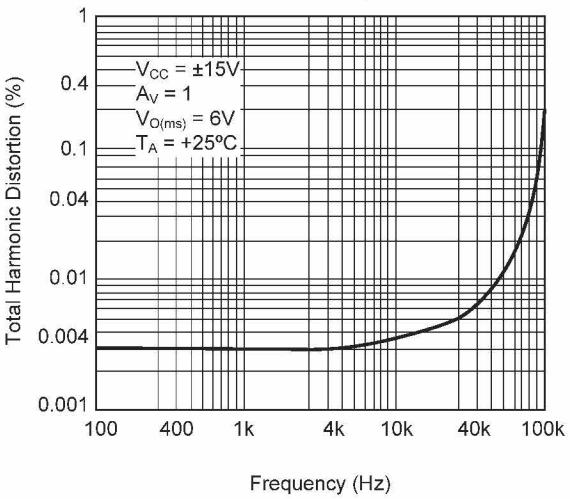
Output Voltage vs. Elapsed Time



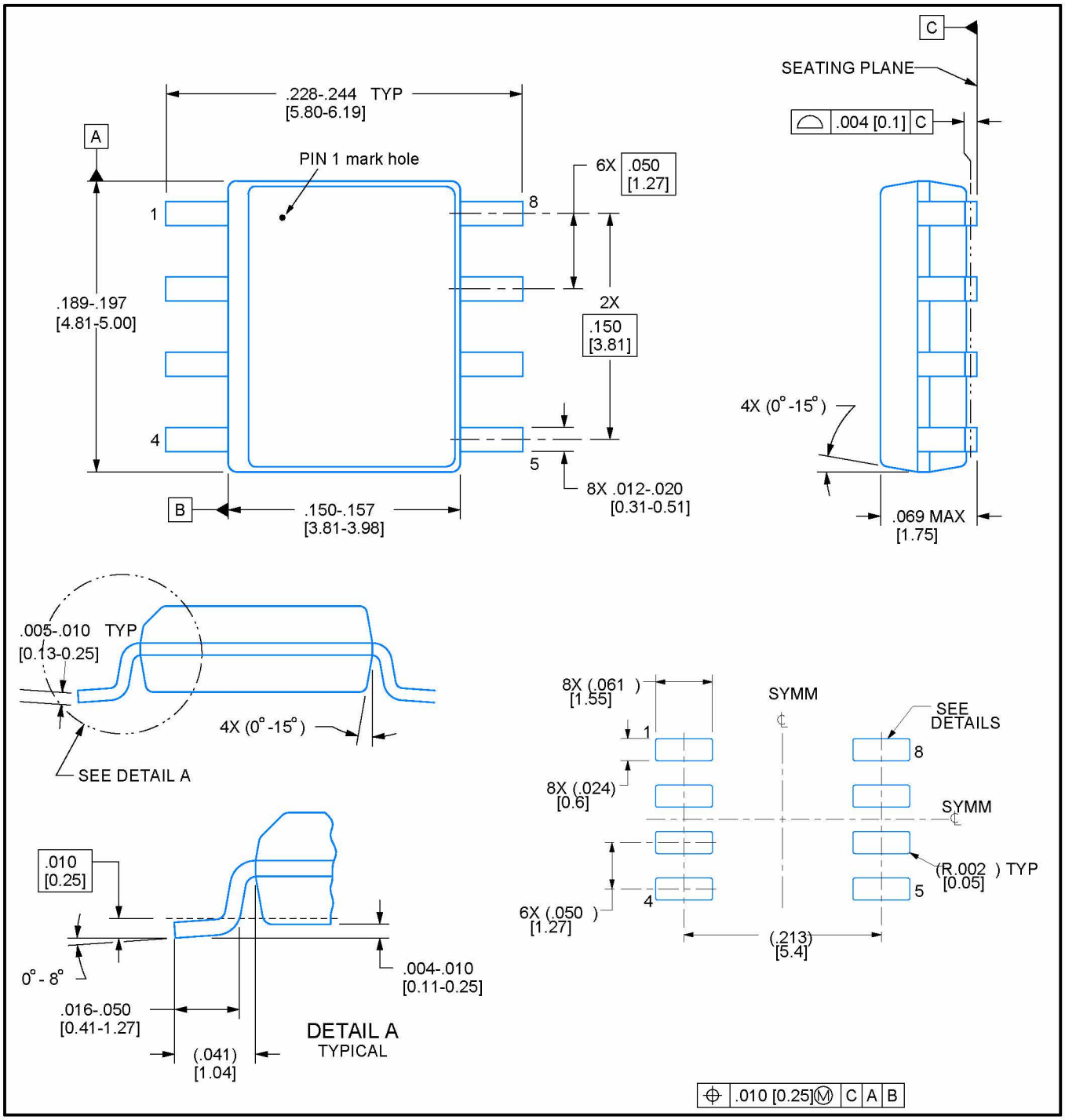
Equivalent Input Noise Voltage vs. Frequency



Total Harmonic Distortion vs. Frequency



PACKAGE OUTLINE SOIC - 8,1.75 mm max height



NOTES: Linear dimensions are in inches [millimeters]. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.