Real-time clock/calendar

1. General description

The TK8563 is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power consumption. A programmable clock output, interrupt output, and voltage-low detector are also provided. All addresses and data are transferred serially via a two-line bidirectional I^2C-bus. Maximum bus speed is 400 kbit/s. The register address is incremented automatically after each written or read data byte.

2. Features and benefits

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Century flag
- Clock operating voltage: 1.0 V to 5.5 V at room temperature
- Low backup current; typical 0.25 μA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 400 kHz two-wire I^2C-bus interface (at V_{DD} = 1.8 V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1.024 kHz, 32 Hz, and 1Hz)
- Alarm and timer functions
- Integrated oscillator capacitor
- Internal Power-On Reset (POR)
- I^2C-bus slave address: read A3h and write A2h
- Open-drain interrupt pin

3. Applications

- Mobile telephones
- Portable instruments
- Electronic metering
- Battery powered products

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TK8563IA	SO8	plastic small outline package; 8 leads; body width 3.9 mm	
TK8563IF	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	

5. Block diagram

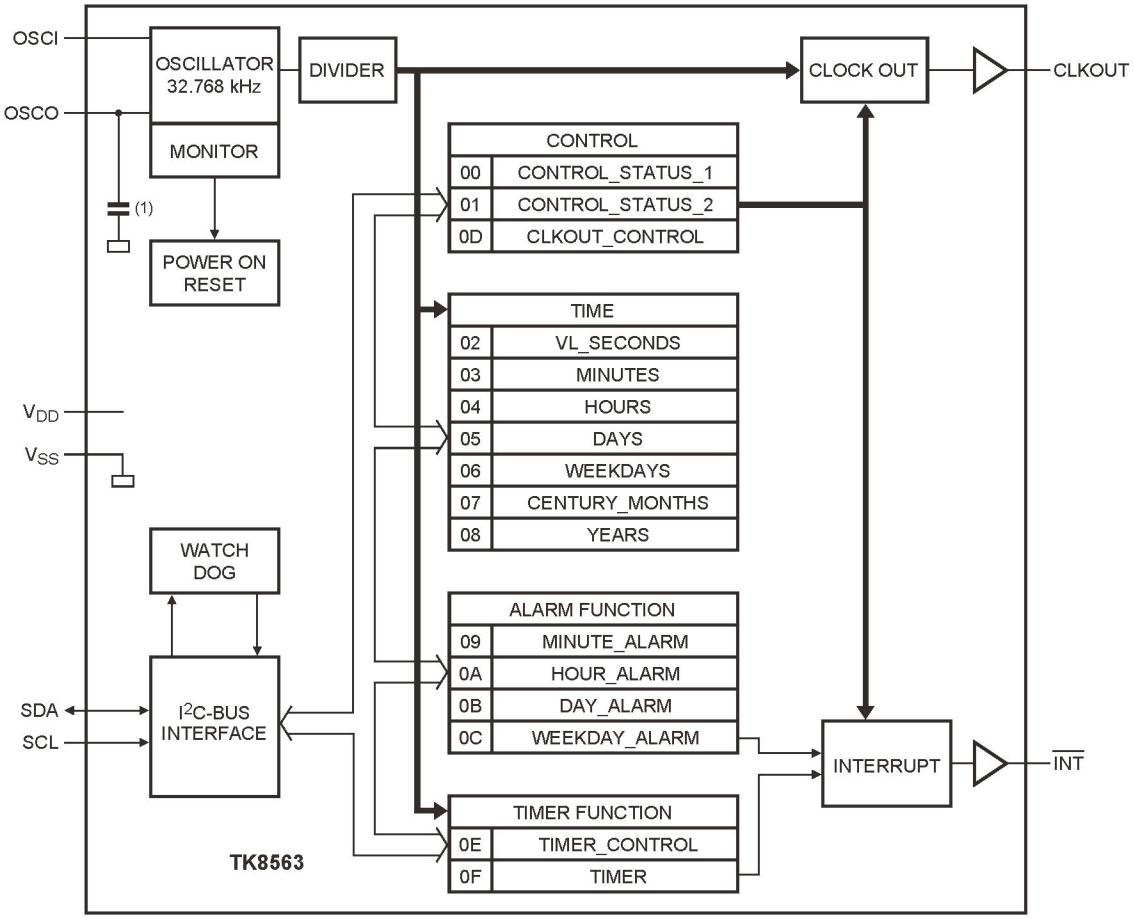
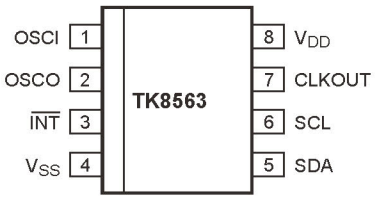


Fig 1. Block diagram of TK8563

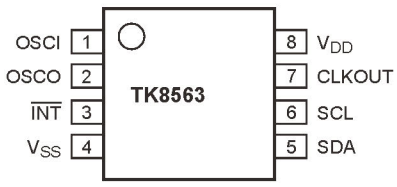
7. Pinning information

7.1 Pinning



Top view.

Fig 3.Pin configuration for SO8



Top view.

Fig 4.Pin configuration for TSSOP8

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO8, TSSOP8	HVSON10	
OSCI	1	1	oscillator input
OSCO	2	2	oscillator output
$\overline{INT}$	3	4	interrupt output (open-drain; active LOW)
V_{SS}	4	[1]5	ground
SDA	5	6	serial data input and output
SCL	6	7	serial clock input
CLKOUT	7	8	clock output, open-drain
V_{DD}	8	9	supply voltage
n.c.	-	3, 10	not connected; do not connect and do not use as feed through

[1] The die paddle (exposed pad) is connected to V_{SS} through high ohmic (non-conductive) silicon attach and should be electrically isolated. It is good engineering practice to solder the exposed pad to an electrically isolated PCB copper pad for better heat transfer but it is not required as the RTC doesn't consume much power. In no case should traces be run under the package exposed pad.

8. Internal circuitry

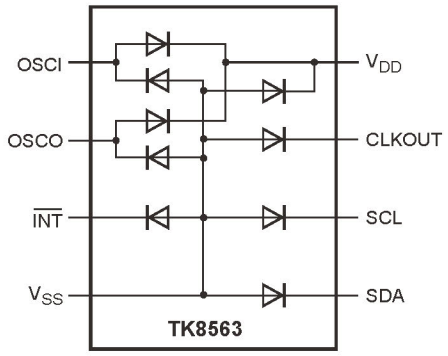


Fig 5. Device diode protection diagram

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		0.5–	+6.5	V
I_{DD}	supply current		50–	+50	mA
V_I	input voltage	on pins SCL, SDA, and OSCI	0.5–	+6.5	V
V_O	output voltage	on pins CLKOUT and $\overline{INT}$	0.5–	+6.5	V
I_I	input current	at any input	10–	+10	mA
I_O	output current	at any output	10–	+10	mA
P_{tot}	total power dissipation		-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM			
		HVSON10 [1]	-	3500±	V
		SO8 [1]			
		TSSOP8 [1]			
		SO8 [1]	-	2000±	V
		TSSOP8 [1]	-		
		CDM	-		
		HVSON10 [2]	-	2000±	V
		SO8 [2]	-	1000±	V
		SO8 [2]	-	1500±	V
		TSSOP8 [2]		1500±	V
		TSSOP8 [2]		1750±	V
I_{lu}	latch-up current	[3]	-	2	mA
T_{stg}	storage temperature	[4]	65–	+150	°C
T_{amb}	ambient temperature	operating device	40–	+85	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 5 "JESD22-A114".

[2] Pass level; Charged-Device Model (CDM), according to Ref. 6 "JESD22-C101".

[3] Pass level; latch-up testing according to Ref. 7 "JESD78" at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the NXP store and transport requirements (see Ref. 9 "UM10569") the devices should be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

10. Static characteristics

Table 5. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage	interface inactive; f_{SCL} = 0 Hz; T_{amb} = 25 °C [1]	1.0	-	5.5	V
		interface active; f_{SCL} = 400 kHz	1.8	-	5.5	V
		clock data integrity; T_{amb} = 25 °C	V_{low}	-	5	V
I_{DD}	supply current	interface active				
		f_{SCL} = 400 kHz	-	-	800	μA
		f_{SCL} = 100 kHz	-	-	200	μA
		interface inactive (f_{SCL} = 0 Hz); CLKOUT disabled; T_{amb} = 25 °C [2]				
		V_{DD} = 5.0 V	-	275	550	nA
		V_{DD} = 3.0 V	-	250	500	nA
		V_{DD} = 2.0 V	-	225	450	nA
		interface inactive (f_{SCL} = 0 Hz); CLKOUT disabled; T_{amb} = −40 °C to + 85 °C [2]				
		V_{DD} = 5.0 V	-	500	750	nA
		V_{DD} = 3.0 V	-	400	650	nA
		V_{DD} = 2.0 V	-	400	600	nA
		interface inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz; T_{amb} = 25 °C [2]				
		V_{DD} = 5.0 V	-	825	1600	nA
		V_{DD} = 3.0 V	-	550	1000	nA
		V_{DD} = 2.0 V	-	425	800	nA
		interface inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz; T_{amb} = −40 °C to + 85 °C [2]				
		V_{DD} = 5.0 V	-	950	1700	nA
		V_{DD} = 3.0 V	-	650	1100	nA
		V_{DD} = 2.0 V	-	500	900	nA
Inputs						
V_{IL}	LOW-level input voltage		0.5−	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	1 −	0	+ 1	μA
C_i	input capacitance	[3]	-	-	7	p

Table 5. Static characteristics *...continued*

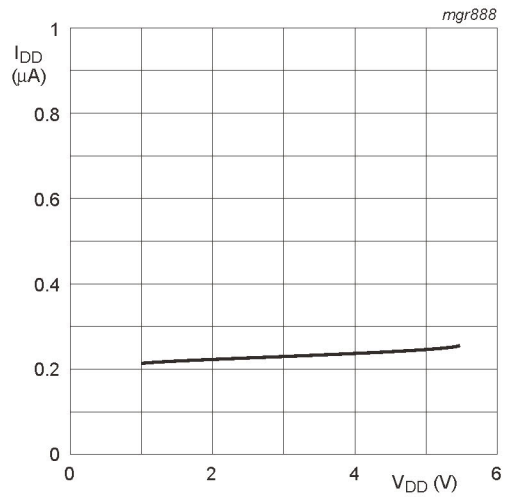
V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Outputs						
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V				
		on pin SDA	3	-	-	mA
		on pin $\overline{INT}$	1	-	-	mA
		on pin CLKOUT	1	-	-	mA
I_{LO}	output leakage current	V_O = V_{DD} or V_{SS}	−1	0	+1	μA
Voltage detector						
V_{low}	low voltage	T_{amb} = 25 °C; sets bit VL; see Figure 6	-	0	1	V

[1] For reliable oscillator start-up at power on use V_{DD} greater than 1.3 V. If powered up at 1.0 V the oscillator will start but it might be a bit slow, especially if at high temperature. Normally the power supply is not 1.0 V at start up and only comes at the end of battery discharge. V_{DD} min of 1.0 V is specified so that the customer can calculate how large a battery or capacitor they need for their application. V_{DD} min of 1.3 V or greater is needed to ensure speedy oscillator start-up time.

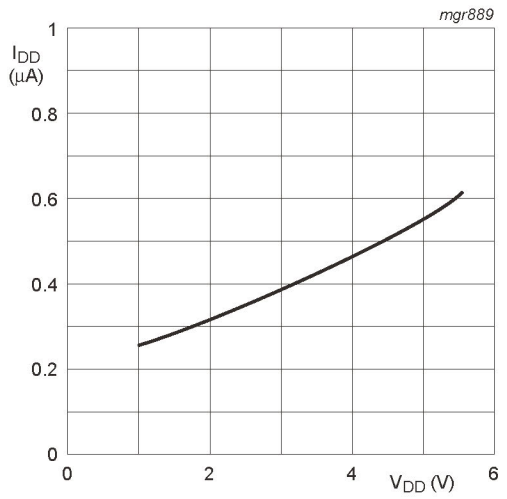
[2] Timer source clock = 1/60 Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.

[3] Tested on sample basis.



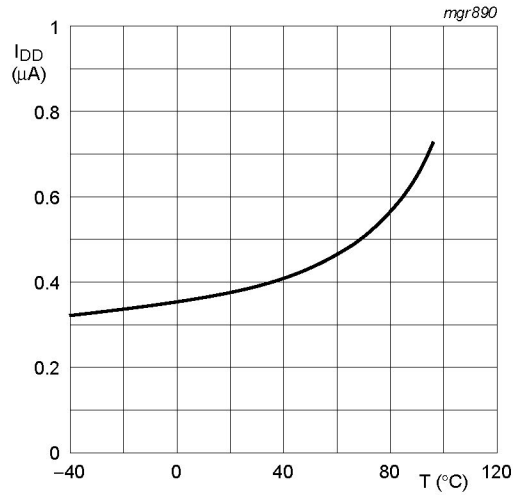
T_{amb} = 25 °C; Timer = 1 minute.

Fig 6. Supply current I_{DD} as a function of supply voltage V_{DD}; CLKOUT disabled



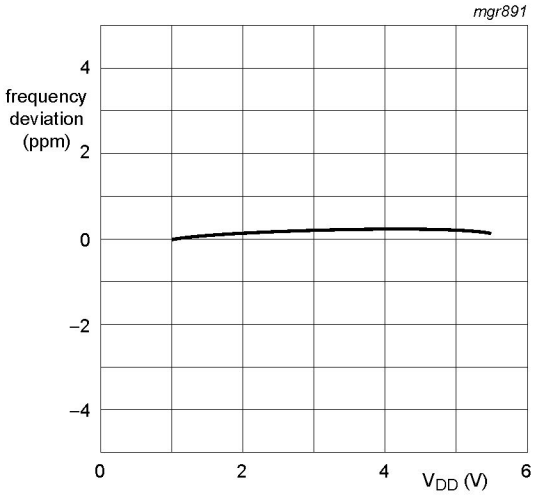
T_{amb} = 25 °C; Timer = 1 minute.

Fig 7. Supply current I_{DD} as a function of supply voltage V_{DD}; CLKOUT = 32 kHz



V_{DD} = 3 V; Timer = 1 minute.

Fig 8. Supply current I_{DD} as a function of temperature T; CLKOUT = 32 kHz



T_{amb} = 2 5 °C; normalized to V_{DD} = 3 V .

Fig 9. Frequency deviation as a function of supply voltage V_{DD}

11. Dynamic characteristics

Table 6. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V ; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 4 0 k Ω; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
C_{OSCO}	capacitance on pin OSCO		15	25	35	pF
$\Delta f_{osc}/f_{osc}$	relative oscillator frequency variation	ΔV_{DD} = 2 0 0 m V ; T_{amb} = 2 5 °C	-	0	-	p2 m
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		-	-	100	kΩ
C_L	load capacitance	parallel [1]	7	-	12.5	pF
C_{trim}	trimmer capacitance	external; on pin OSCI	5	-	2	5
CLKOUT output						
δ_{CLKOUT}	duty cycle on pin CLKOUT	[2]	-	5	-0	%
I^2C-bus timing characteristics (see Figure 27)[3][4]						
f_{SCL}	SCL clock frequency	[5]	-	-	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	μs
t_{LOW}	LOW period of the SCL clock		1.3	-	-	μs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	μs
t_r	rise time of both SDA and SCL signals					
		standard-mode	-	-	1	μs
		fast-mode	-	-	0.3	μs

Table 6. Dynamic characteristics *...continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
$t_{w(spike)}$	spike pulse width	on bus	-	-	50	ns

[1] C_L is a calculation of C_{trim} and C_{OSCO} in series: $C_L = \frac{C_{trim} \cdot C_{OSCO}}{C_{trim} + C_{OSCO}}$.

[2] Unspecified for f_{CLKOUT} = 32.768 kHz.

[3] All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[4] A detailed description of the I²C-bus specification is given in Ref. 11 “UM10204”.

[5] I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

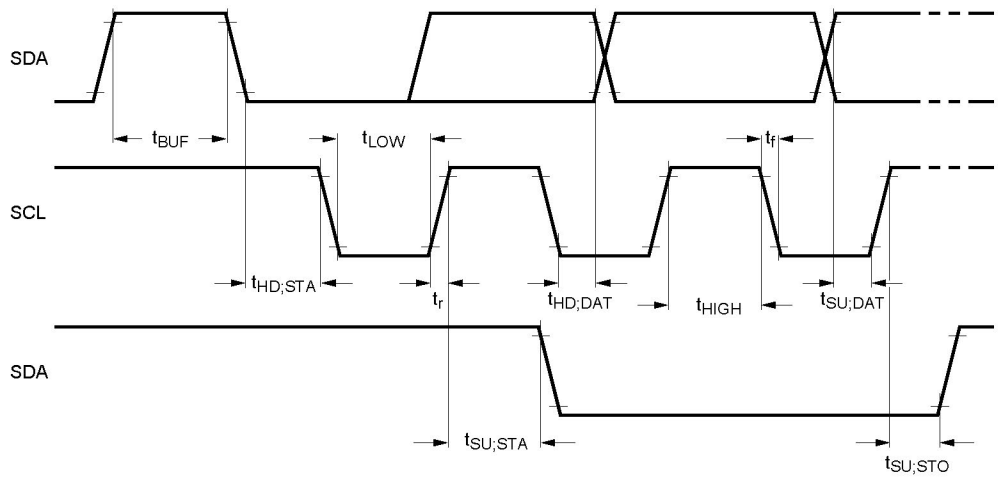


Fig 10. I²C-bus timing waveforms

12. Application information

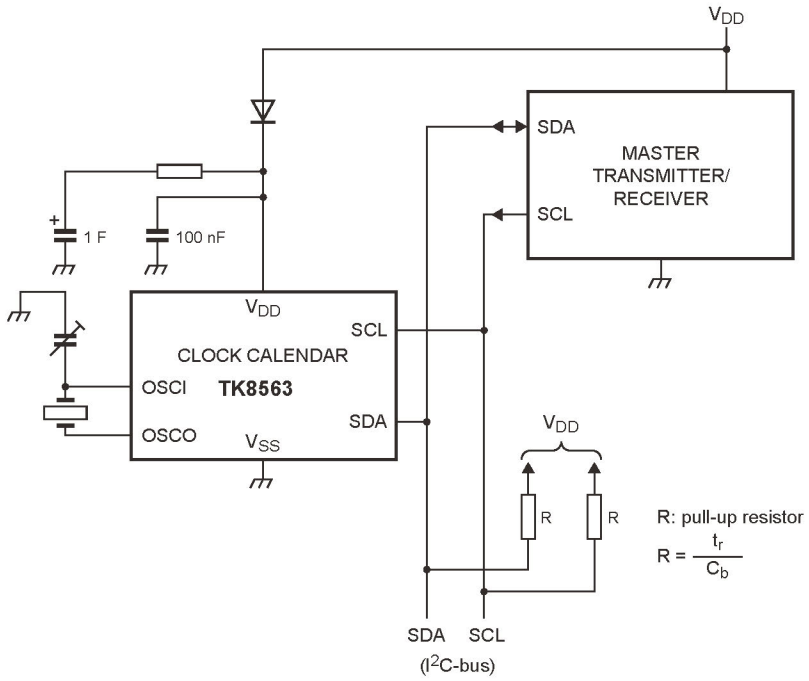


Fig 11. Application diagram

12.1 Quartz frequency adjustment

12.1.1 Method 1: fixed OSCI capacitor

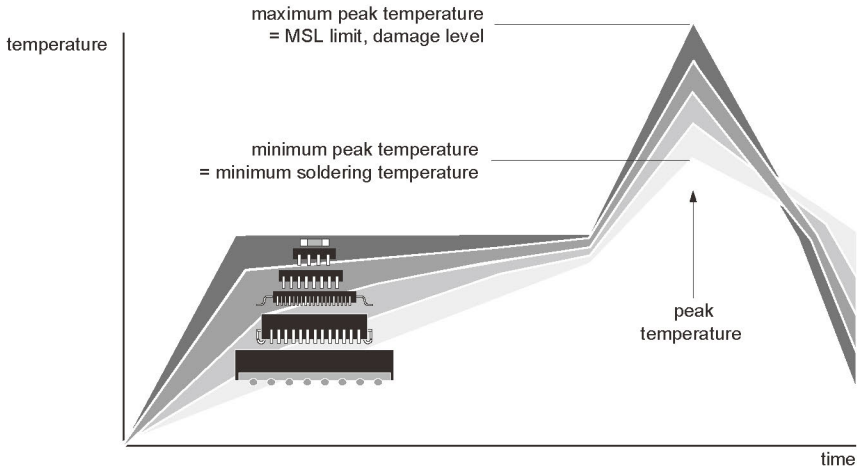
By evaluating the average capacitance necessary for the application layout, a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at pin CLKOUT. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average ±5 ppm). Average deviations of ±5 minutes per year can be easily achieved.

12.1.2 Method 2: OSCI trimmer

Using the 32.768 kHz signal available after power-on at pin CLKOUT, fast setting of a trimmer is possible.

12.1.3 Method 3: OSCO output

Direct measurement of OSCO out (accounting for test probe capacitance).



MSL: Moisture Sensitivity Level

Fig 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.