ZERO-DRIFT, SINGLE-SUPPLY, RAIL-TO-RAIL INPUT/ OUTPUT CMOS OPERATIONAL AMPLIFIERS

■ Description

The TTESEMI TK8554 has ultralow offset, drift, and bias current. The TK8554 is dual amplifiers featuring rail-to-rail input and output swings. Single supply as low as 2.7V and up to 5V may be used.

With an offset voltage of only 1μV. The TK8554 is perfectly suited for applications in which error sources cannot be tolerated. Position and pressure sensors and strain gage amplifiers benefit greatly from nearly zero drift. The rail-to-rail input and output swings provided by the TK8554 make both high-side and low-side sensing easy.

■ Features

* Single-supply operation: 2.7V~5.0V
* Low offset voltage: 1μV
* Rail-to-rail input and output swing
* No external capacitors required

■ Applications

* Temperature sensors
* Pressure sensors
* Precision current sensing
* Strain gage amplifiers
* Medical instrumentation
* Thermocouple amplifiers

■ Ordering Information

Ordering Number	Package	Packing
TK8554ARUZ	TSSOP-14	Tape Reel
TK8554ARZ	SOIC-14	Tape Reel

For other encapsulation type products, please contact us.

■ Pin Assignment

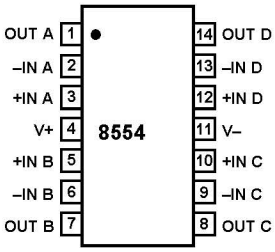


Fig1 14-Lead SOIC and 14-Lead TSSOP

PIN NO.	PIN NAME	DESCRIPTION
1	OUT A	Output pin of A AMP
2	-IN A	Inverting input pin of A AMP
3	+IN A	Non-inverting input of A AMP
4	V+	Positive power supply
5	+IN B	Non-inverting input of B AMP
6	-IN B	Inverting input pin of B AMP
7	OUT B	Output pin of B AMP
8	OUT C	Output pin of C AMP
9	-IN C	Inverting input pin of C AMP
10	+IN C	Non-inverting input of C AMP
11	V-	Negative power supply
12	+IN D	Non-inverting input of D AMP
13	-IN D	Inverting input pin of D AMP
14	OUT D	Output pin of D AMP

■ Functional Diagram

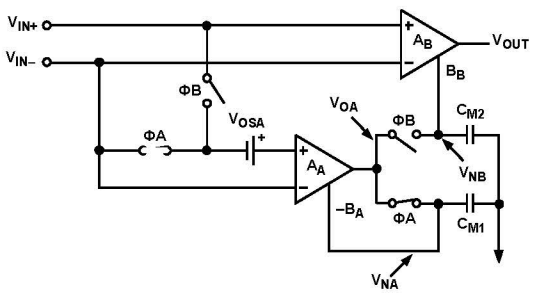


Fig2 Auto-Zero Phase of the TK8554

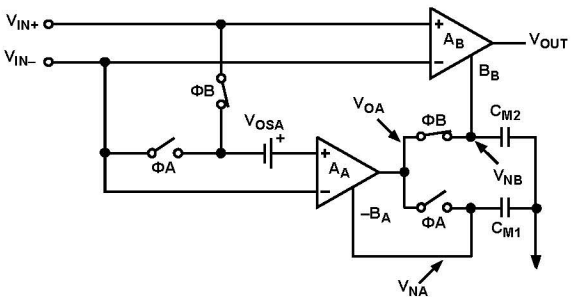


Fig3 Output Phase of the Amplifier

■ Block Diagram

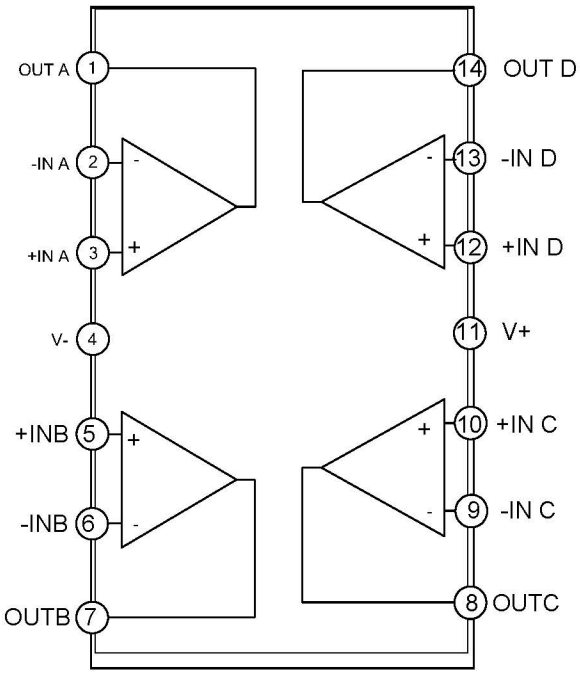


Fig 4 Block Diagram for TK8554

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	6	V
Input Voltage	V_{IN}	GND - 0.3 ~ V_S + 0.3	V
Differential Input Voltage (Note 2)	V_{ID}	±5	V
Junction Temperature Range	T_J	+150	°C
Operating Temperature Range	T_{OPR}	-40 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Different I input voltage is limited to ±5.0 V or the supply voltage, whichever is less.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	180	°C/W
Junction to Case	θ_{JC}	43	°C/W

■ ELECTRICAL CHARACTERISTICS

VS=5.0V, VCM=2.5V, VO=2.5V, TA=25°C unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	20	μV
Input Bias Current	I_B			1.0	1.5	nA
Input Offset Current	I_{OS}			150		pA
Input Voltage Range	V_I		0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=0V~+5V	10	120		dB
Large Signal Voltage Gain (Note)	A_{VO}	R_L=10kΩ, V_O=0.3V~4.7V	98	125		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L=100kΩ to Ground	4.99	4.998		V
		R_L=10kΩ to Ground	4.95	4.98		V
Output Voltage Low	V_{OL}	R_L=100kΩ to V+		1	10	mV
		R_L=10kΩ to V+		10	30	mV
Output Short-Circuit Limit Current	I_{SC}		±25	±65		mA
Output Current	I_O			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S=2.7V~5.5V		110		dB
Supply Current/Amplifier	I_{SY}	V_O=0V		650	1000	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L=10kΩ		0.33		V/μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			1.2		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0Hz~10Hz		1.0		μV p-p
		0Hz~1Hz		0.32		μV p-p
Voltage Noise Density	e_n	f=1kHz		42		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f=10Hz		2		$fA/\sqrt{Hz}$

Note: Gain testing is dependent upon test bandwidth.

■ ELECTRICAL CHARACTERISTICS (Cont.)

(VS=2.7V, VCM=1.35V, VO=1.35V, TA=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	20	μV
Input Bias Current	I_B			1.0	1.5	nA
Input Offset Current	I_{OS}			150		pA
Input Voltage Range	V_I		0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=0V~+2.7V		120		dB
Large Signal Voltage Gain (Note)	A_{VO}	R_L=10kΩ, V_O=0.3V~2.4V	98	125		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L=100kΩ to Ground	2.685	2.697		V
		R_L=10kΩ to Ground	2.67	2.68		V
Output Voltage Low	V_{OL}	R_L=100kΩ to V+		1	10	mV
		R_L=10kΩ to V+		10	20	mV
Output Short-Circuit Limit Current	I_{SC}		±10	±20		mA
Output Current	I_O			±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S=2.7V~5.5V		110		dB
Supply Current/Amplifier	I_{SY}	V_O=0V		600	900	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L=10kΩ		0.4		V/μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			1		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0Hz~10Hz		1.6		μV p-p
Voltage Noise Density	e_n	f=1kHz		75		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f=10Hz		2		fA/$\sqrt{Hz}$

Note: Gain testing is dependent upon test bandwidth.

■ TYPICAL PERFORMANCE CHARACTERISTICS

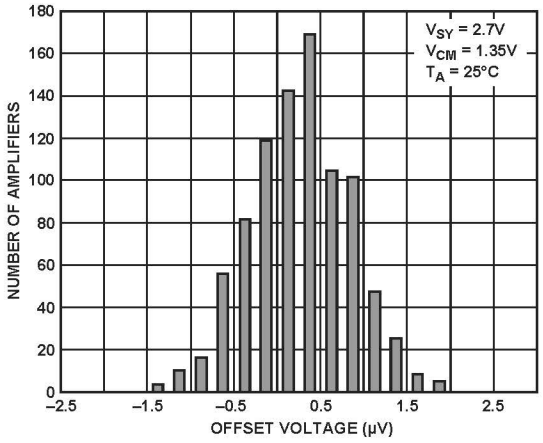


Figure 5. Input Offset Voltage Distribution at 2.7 V

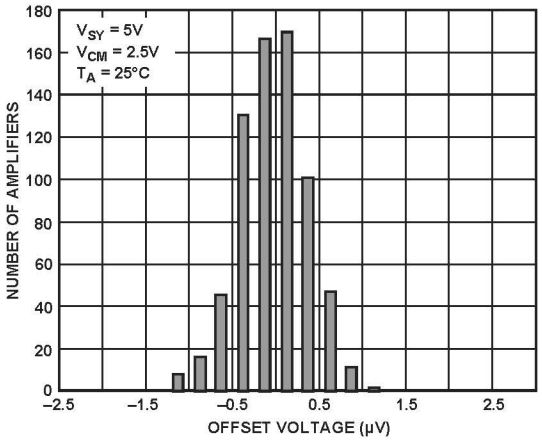


Figure 8. Input Offset Voltage Distribution at 5 V

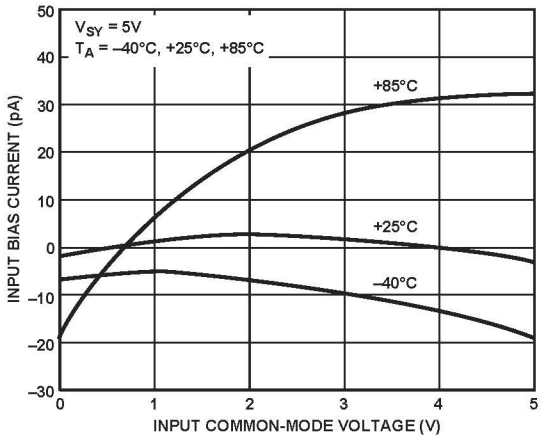


Figure 6. Input Bias Current vs. Common-Mode Voltage

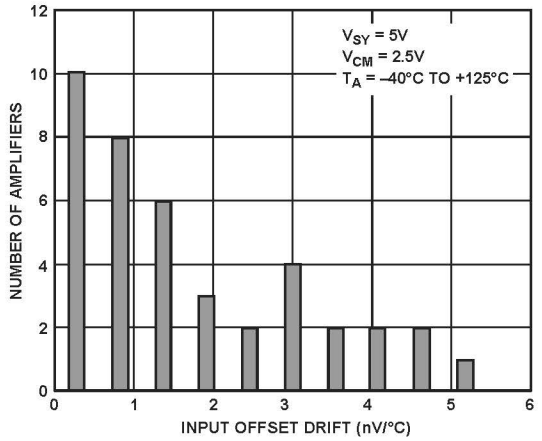


Figure 9. Input Offset Voltage Drift Distribution at 5 V

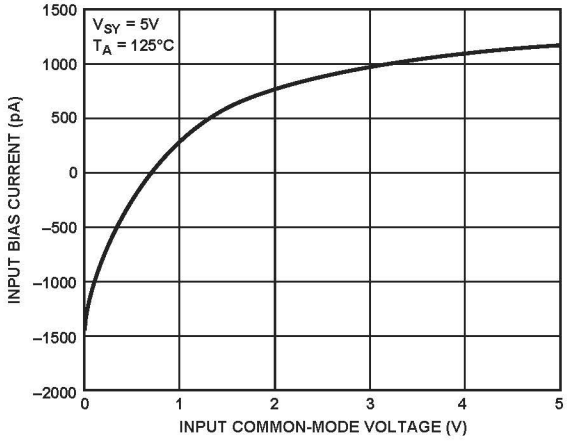


Figure 7. Input Bias Current vs. Common-Mode Voltage

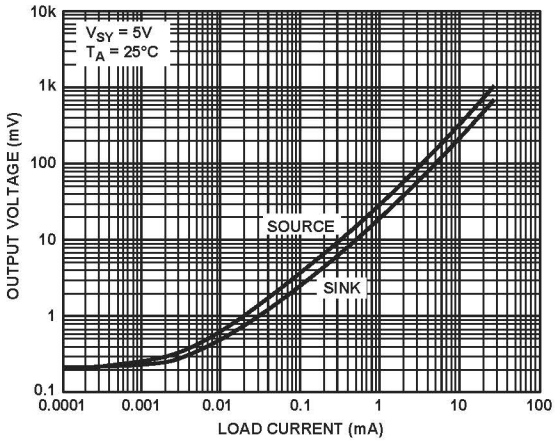


Figure 10. Output Voltage to Supply Rail vs. Load Current at 5 V

■ TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

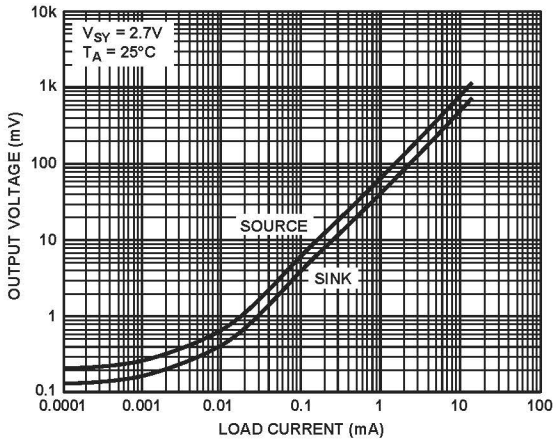


Figure 11. Output Voltage to Supply Rail vs. Load Current at 2.7 V

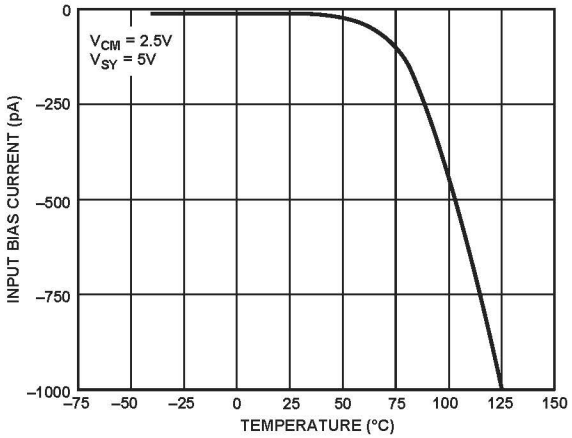


Figure 12. Input Bias Current vs. Temperature

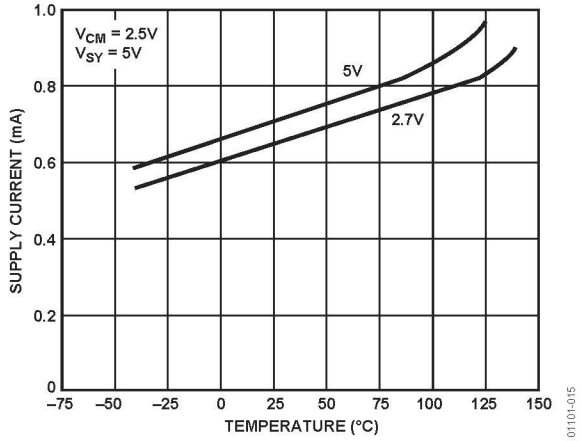


Figure 13. Supply Current vs. Temperature

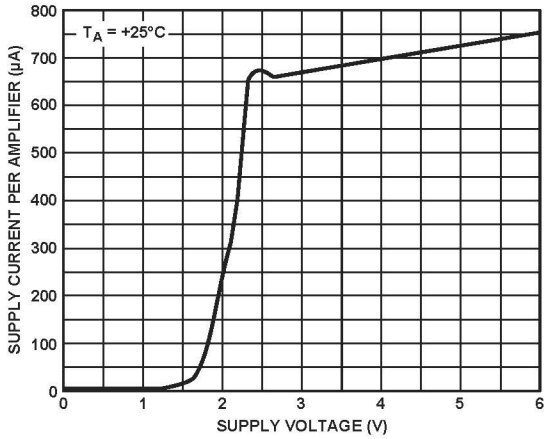


Figure 14. Supply Current per Amplifier vs. Supply Voltage

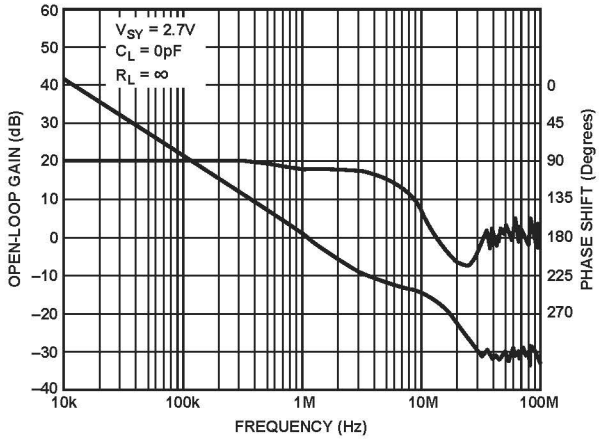


Figure 15. Open-Loop Gain and Phase Shift vs. Frequency at 2.7 V

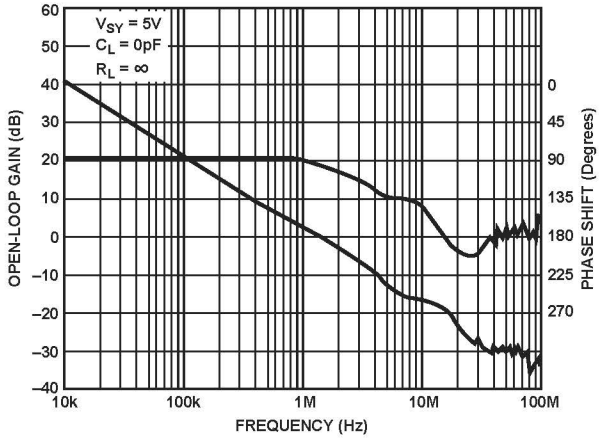


Figure 16. Open-Loop Gain and Phase Shift vs. Frequency at 5 V

■ TYPICAL PERFORMANCE CHARACTERISTICS(Cont.)

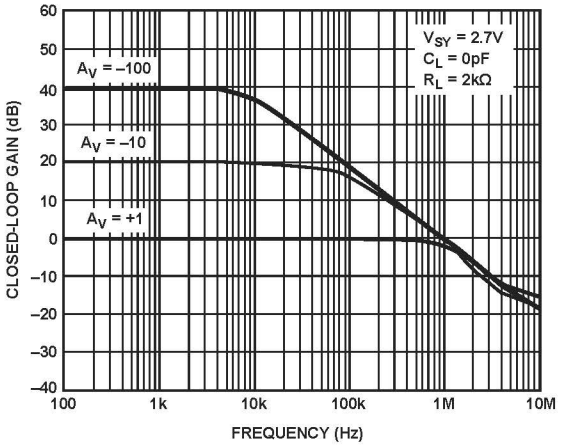


Figure 17. Closed-Loop Gain vs. Frequency at 2.7 V

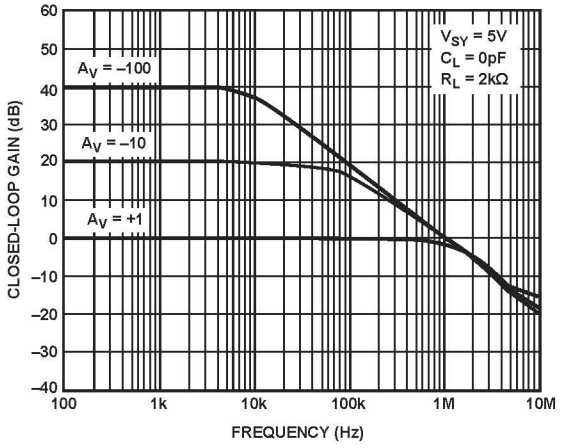


Figure 18. Closed-Loop Gain vs. Frequency at 5 V

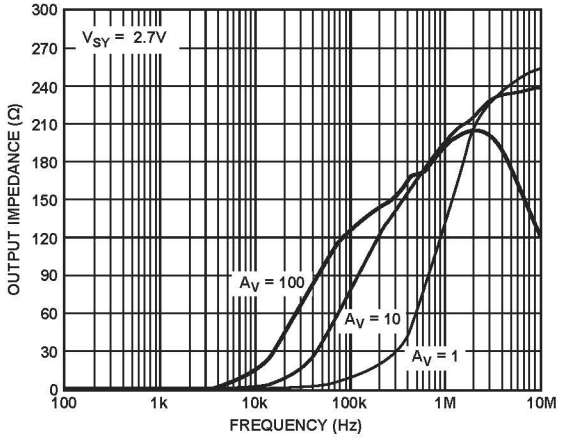


Figure 19. Output Impedance vs. Frequency at 2.7 V

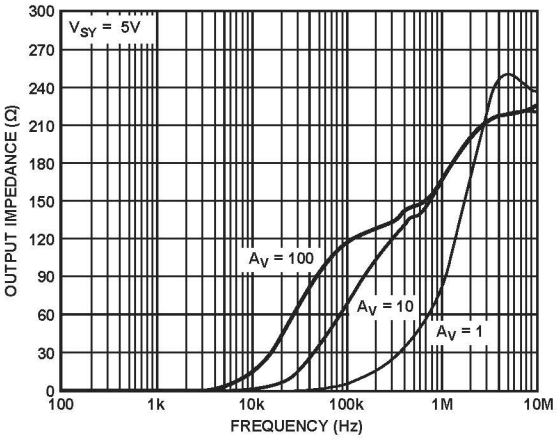


Figure 20. Output Impedance vs. Frequency at 5 V

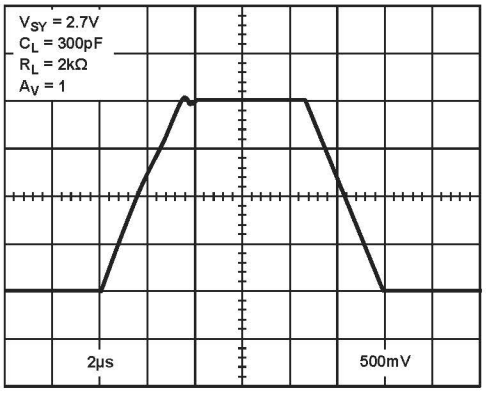


Figure 21. Large Signal Transient Response at 2.7 V

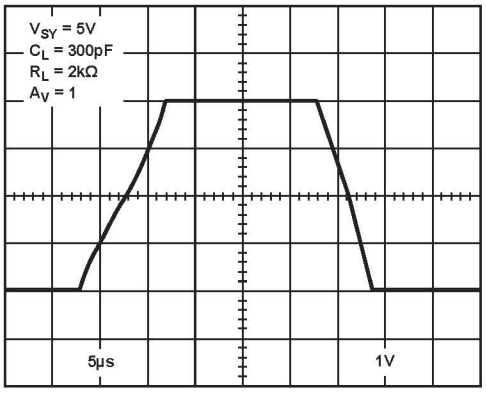
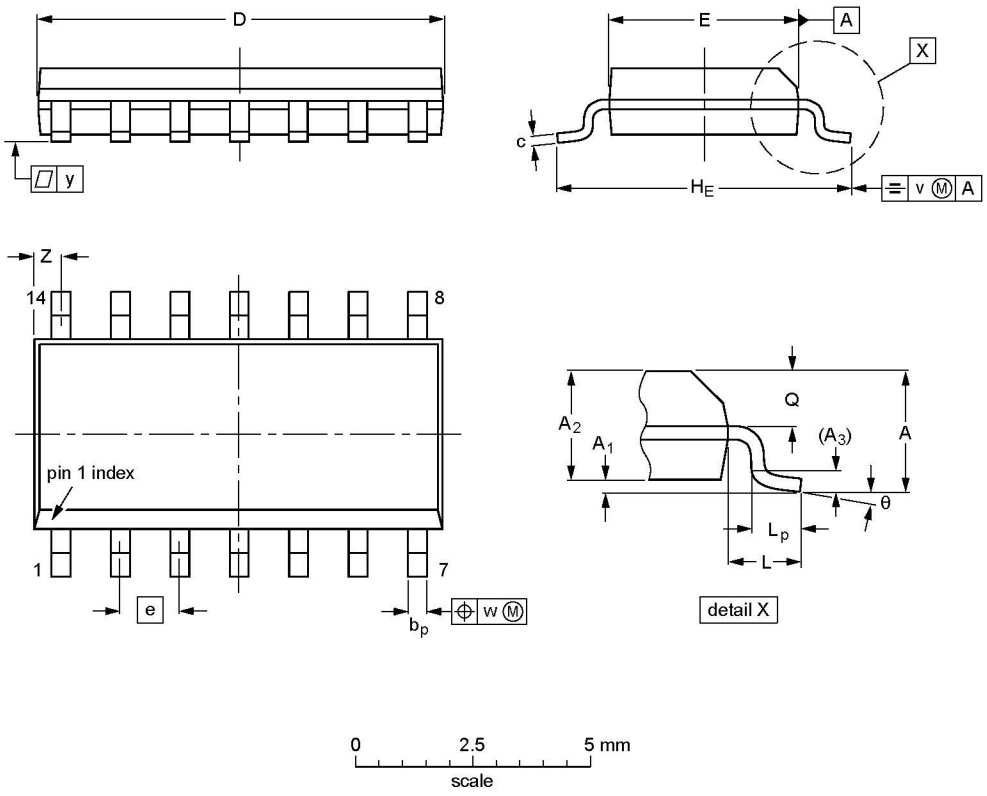


Figure 22. Large Signal Transient Response at 5 V

Package diagram

SOIC14: plastic small outline package; 14 leads; body width 3.9 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TKSOIC14						05-06-19