Low Cost, 0.5 mA Output, Single-Supply Amplifiers

■ Description

The TK8532 is dual rail-to-rail input/output single-supply amplifiers featuring 0.5 mA output drive current. This high output current makes these amplifiers excellent for driving either resistive or capacitive loads. AC performance is very good with 1 MHz bandwidth, 0.55 V/μs slew rate, and low distortion. All are guaranteed to operate from a 1.8 V single supply as well as a 6 V supply.

The very low input bias currents enable the TK8532 to be used for integrators, diode amplification, and other applications requiring low input bias current. Supply current is only 750 μA per amplifier at 5 V, allowing low current applications to control high current loads. Applications include audio amplification for computers, sound ports, sound cards, and set-top boxes. The TK8532 is very stable, and it is capable of driving heavy capacitive loads such as those found in LCDs.

The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs, or other wide output swing devices in single-supply systems.

■ Features

* Single-supply operation: 1.8 V to 6 V
* High output current: ±0.5 mA
* Low supply current: 750 μA/amplifier
* No phase reversal
* Low input currents
* Wide bandwidth: 1 MHz
* Slew rate: 0.55V/μs
* Unity gain stable
* Rail-to-rail input and output

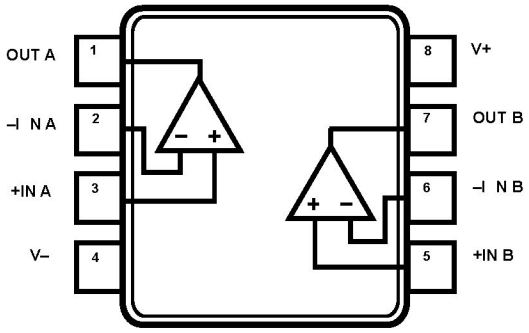
■ Applications

* Multimedia audio
* ASIC input or output amplifiers
* LCD drivers
* Headphone drivers

■ Ordering Information

Ordering Number	Package	Packing
TK8532ARUZ	TSSOP-8	Tape Reel
TK8532ARZ	SOIC-8	Tape Reel

■ Pin Assignment



TK8532 *Fig1.*
8-Lead SOIC and 8-Lead TSSOP

PIN		I/O	DESCRIPTION
NAME	SOIC,TSSOP		
-IN A	2	I	Negative input
+IN A	3	I	Positive input
–IN B	6	I	Negative input
+IN B	5	I	Positive input
OUT A	1	O	Output
OUT B	7	O	Output
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

■ Typical Application

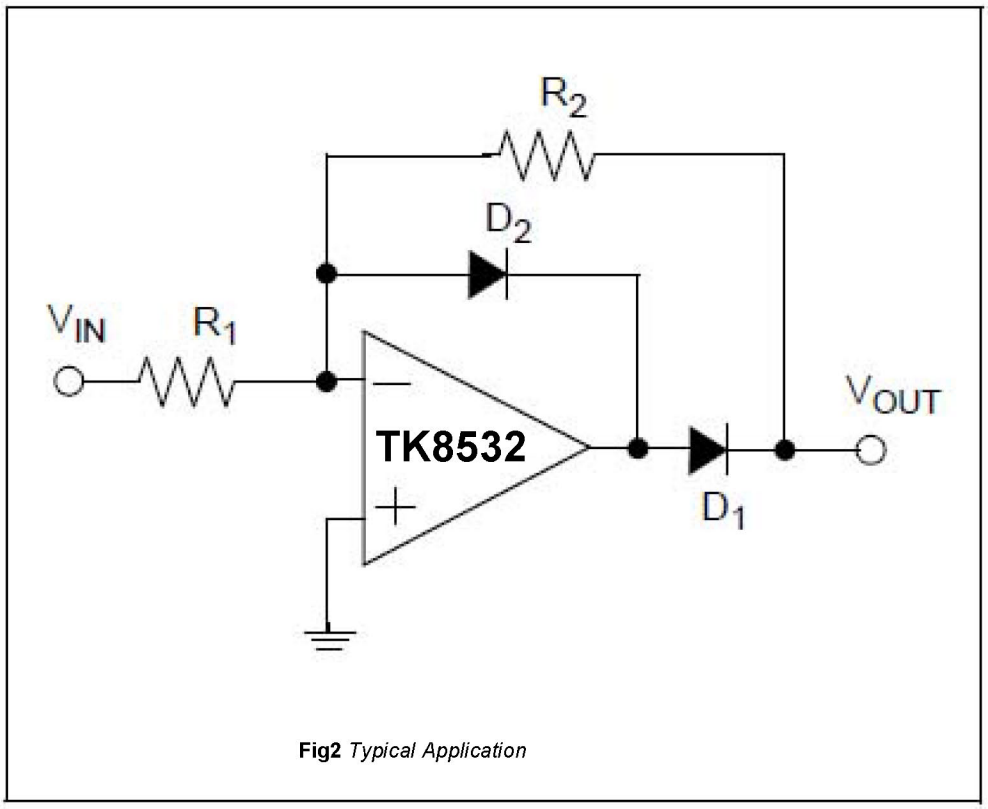


Fig2 *Typical Application*

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

Parameter	Rating
Supply Voltage (V_S)	7 V
Input Voltage	GND to V_S
Differential Input Voltage	±6 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Protection on All Pins(HBM;MM;CDM)	14KV,300V,1500V

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOIC-8	θ_{JA}	158	°C/W
	Tssop-8	θ_{JA}	153	

■ ELECTRICAL CHARACTERISTICS

(V_S = 2.0 V, V_{CM} = 1.5 V, TA = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	−40°C ≤ T_A ≤ +125°C			25	mV
					30	mV
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C		5	50	pA
					60	pA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C		1	25	pA
					30	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2 V	38	45		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 2V		25		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ TA ≤ +125°C		20		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA −40°C ≤ T_A ≤	1.85	1.92		V
		+125°C I_L = 10 mA	1.8			V
Output Voltage Low	V_{OL}	−40°C ≤ T_A ≤ +125°C		60	100	mV
					125	mV
Output Current	I_{OUT}			±250		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		60		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2 V to 6 V	45	55		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		0.70	1	mA
		−40°C ≤ T_A ≤ +125°C			1.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.5		V/µs
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			1		MHz
Phase Margin	ϕo			70		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

■ ELECTRICAL CHARACTERISTICS (Cont.)

(V_S = 5.0 V, V_{CM} = 2.5 V, TA = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	−40°C ≤ T_A ≤ +125°C			25	mV
					30	mV
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C		5	50	pA
					60	pA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C		1	25	pA
					30	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	38	47		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	15	80		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C T_A≤ ≤+125°C		20		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA	4.9	4.94		V
		−40°C ≤ T_A ≤ +125°C	4.85			V
Output Voltage Low	V_{OL}	I_L = 10 mA		50	100	mV
		−40°C ≤ T_A ≤ +125°C			125	mV
Output Current	I_{OUT}			±250		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		40		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 6 V	45	55		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		0.75	1.25	mA
		−40°C ≤ T_A ≤ +125°C			1.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.55		V/µs
Full-Power Bandwidth	BW_p	1% distortion		350		kHz
Settling Time	t_S	To 0.01%		1.4		µs
Gain Bandwidth Product	GBP			1.1		MHz
Phase Margin	ϕo			70		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

■ TYPICAL PERFORMANCE CHARACTERISTICS

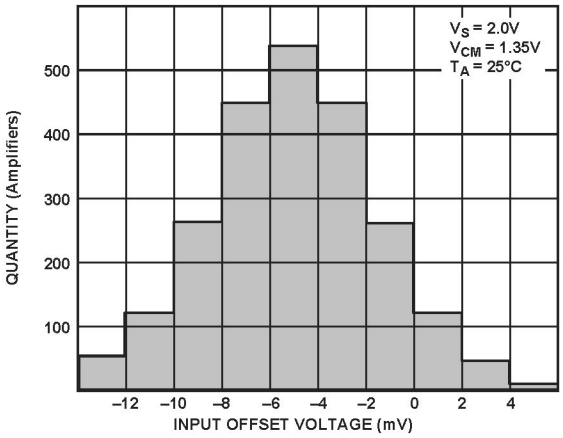


Fig 3. Input Offset Voltage Distribution

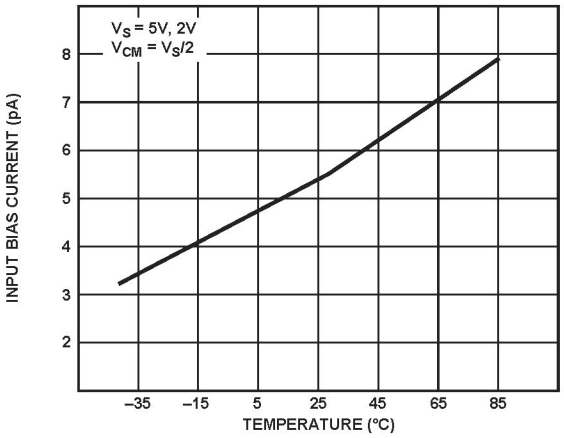


Fig6. Input Bias Current vs. Temperature

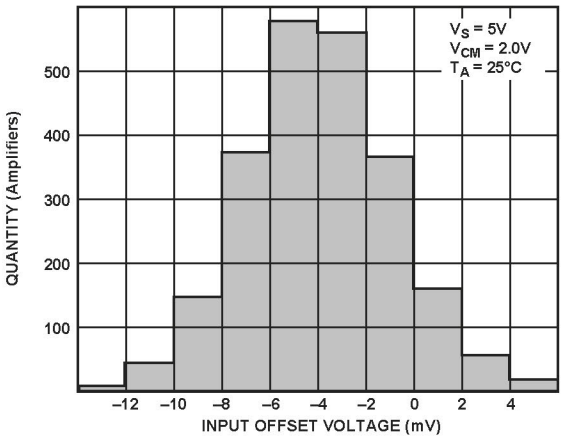


Fig 4. Input Offset Voltage Distribution

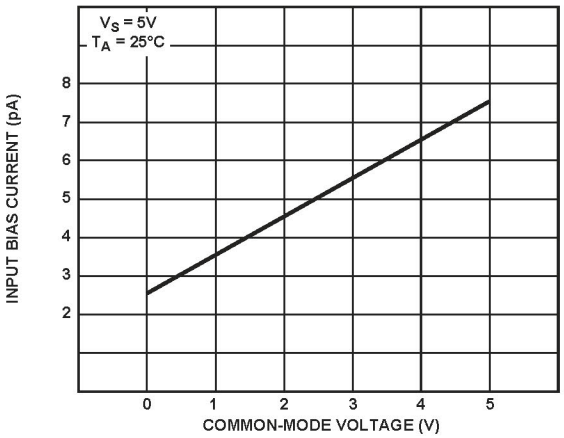


Fig7. Input Bias Current vs. Common-Mode Voltage

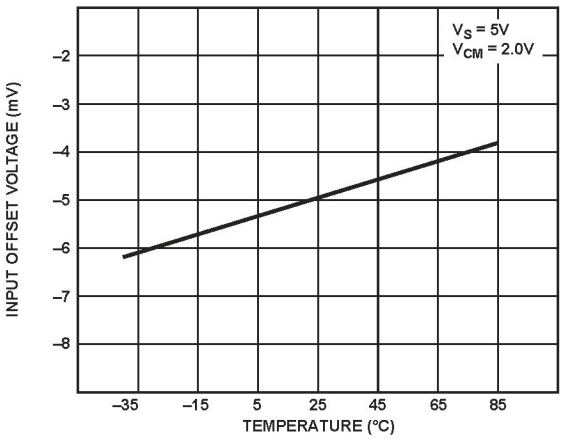


Fig5. Input Offset Voltage vs. Temperature

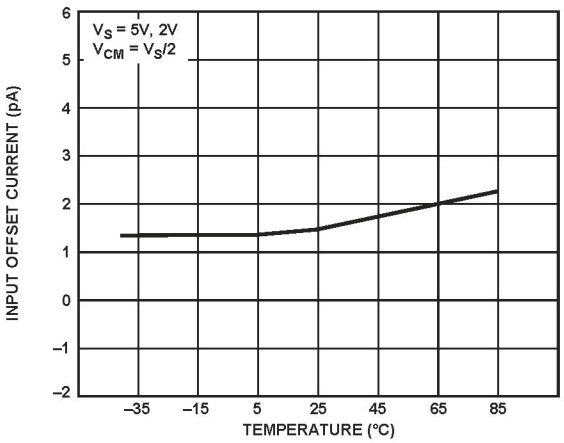


Fig8. Input Offset Current vs. Temperature

■ TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

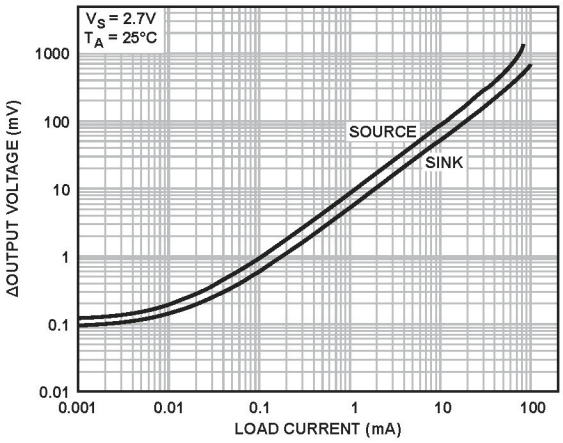


Fig9. Output Voltage to Supply Rail vs. Load Current

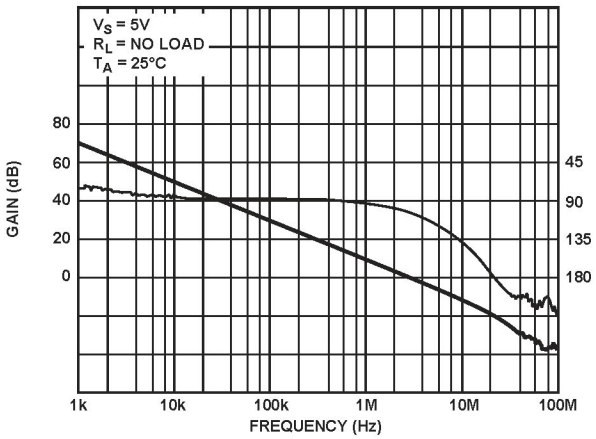


Fig12. Open-Loop Gain and Phase Shift vs. Frequency

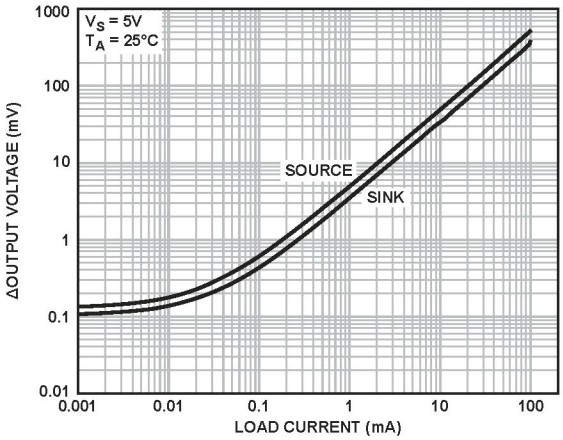


Fig10. Output Voltage to Supply Rail vs. Load Current

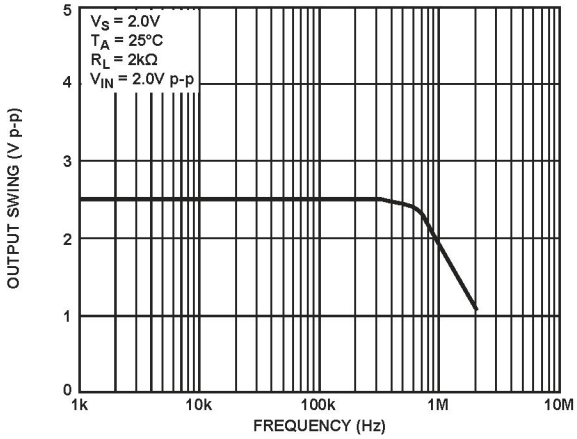


Fig13. Closed-Loop Output Swing vs. Frequency

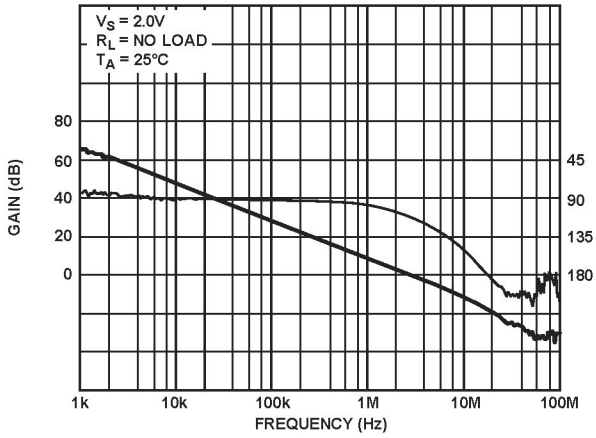


Fig11. Open-Loop Gain and Phase Shift vs. Frequency

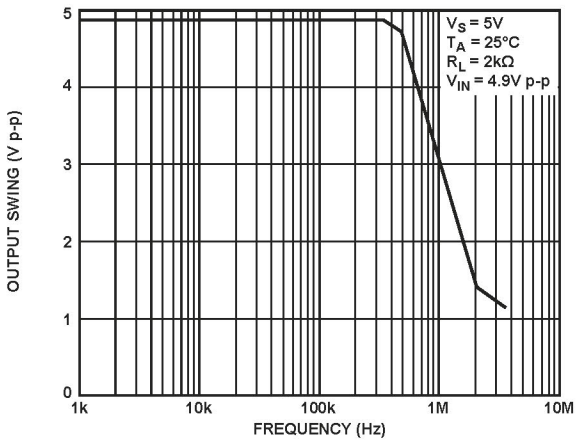


Fig14. Closed-Loop Output Swing vs. Frequency

■ TYPICAL PERFORMANCE CHARACTERISTICS(Cont.)

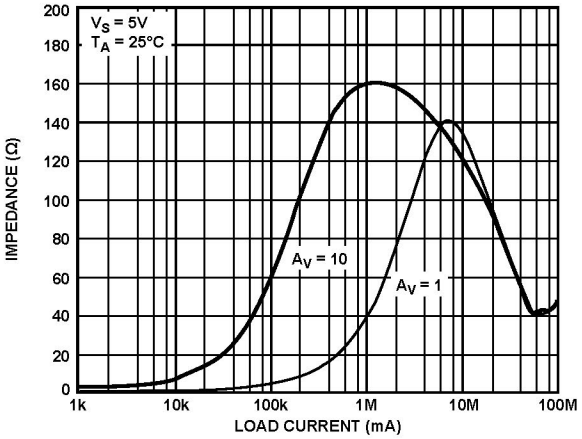


Fig15. Closed-Loop Output Impedance vs. Frequency

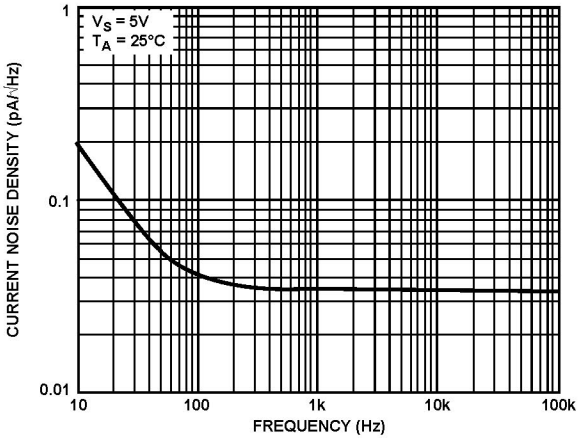


Fig18. Current Noise Density vs. Frequency

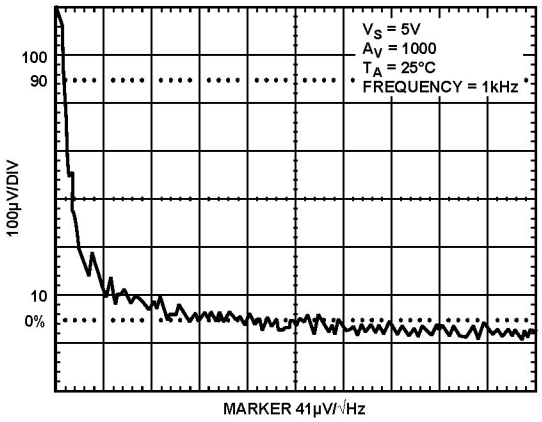


Fig16. Voltage Noise Density vs. Frequency (1 kHz)

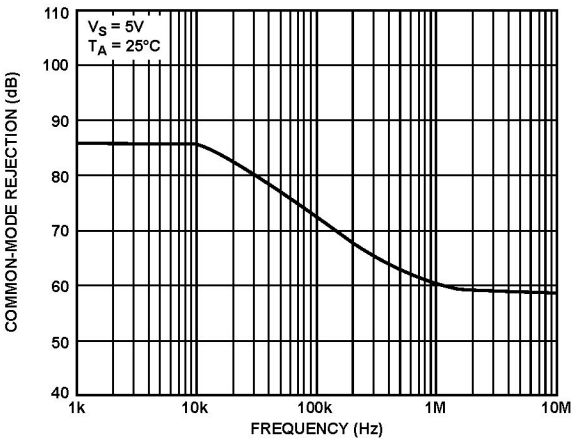


Fig19. Common-Mode Rejection vs. Frequency

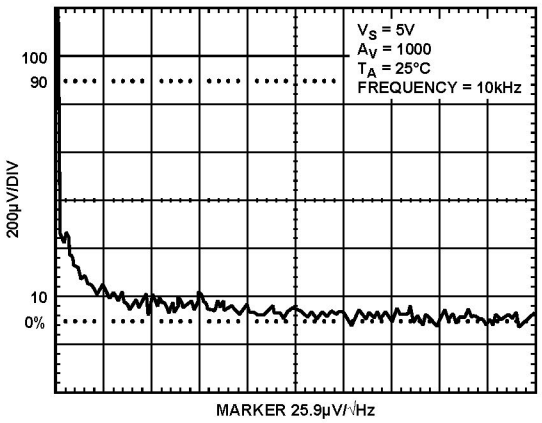


Fig17. Voltage Noise Density vs. Frequency (10 kHz)

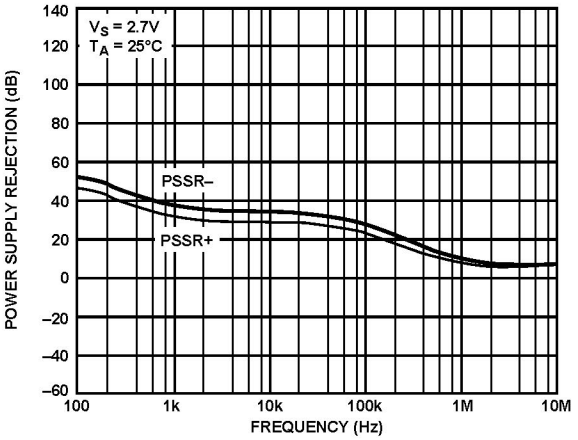
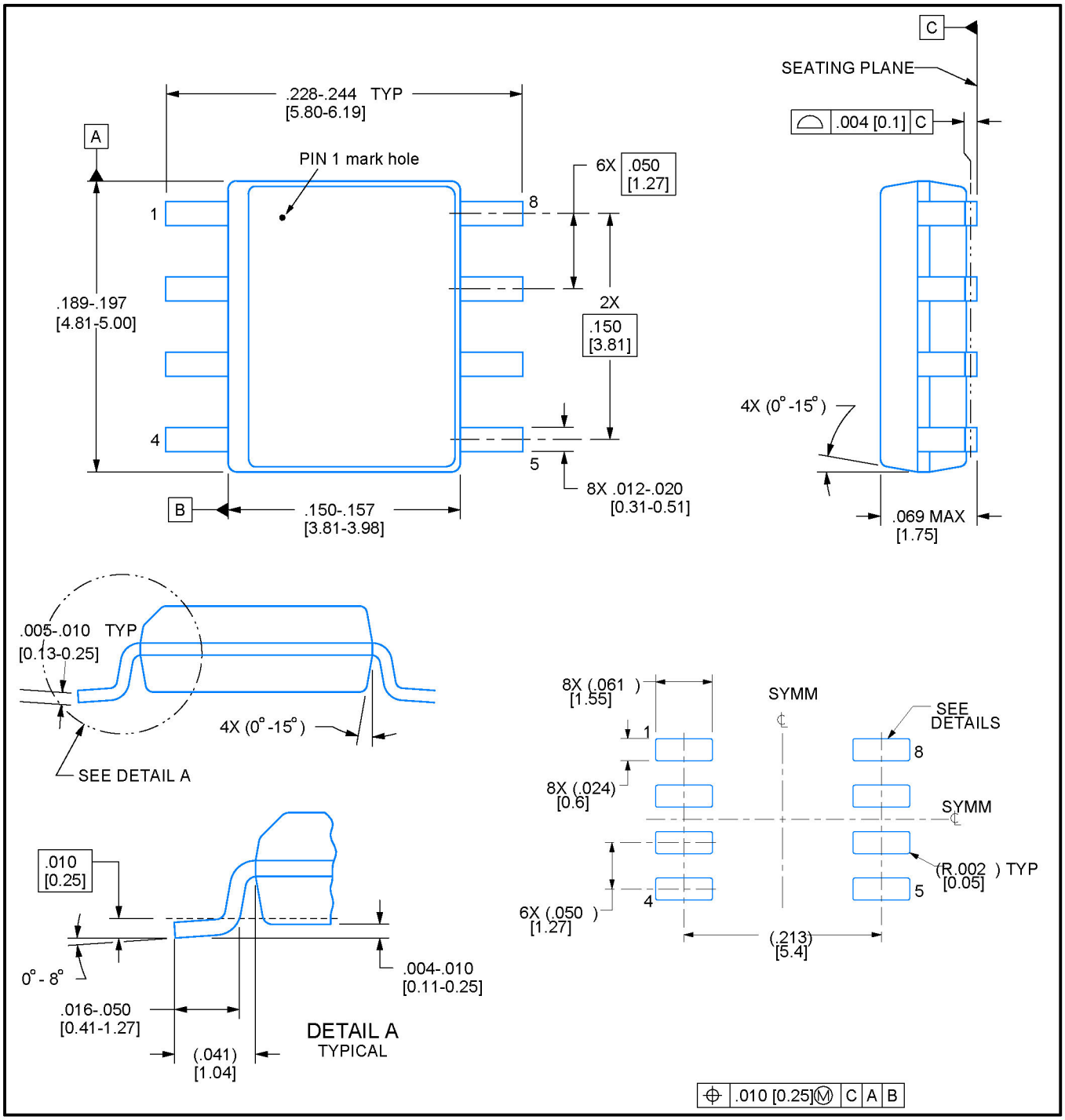


Fig20. Power Supply Rejection vs. Frequency

PACKAGE OUTLINE SOIC - 8,1.75 mm max height



NOTES: Linear dimensions are in inches [millimeters]. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 0.15 per side.