4-Pin µP Voltage Monitors with Manual Reset Input

■ DESCRIPTION

The TK812 is low-power microprocessor (µP) supervisory circuits used to monitor power supplies in µP and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5Vpowered or 3V-powered circuits. The TK812 also provides a debounced manual reset input.

The device perform a single function: It asserts a reset signal whenever the V_{CC} supply voltage falls below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The only difference between the two devices is that the TK811 has an active-low RESET output (which is guaranteed to be in the correct state for VCC down to 1V), while the TK812 has an active-high RESET output. The reset comparator is designed to ignore fast transients on VCC. Reset thresholds are available for operation with a variety of supply voltages.

■ FEATURES

Integrated Voltage Monitor Increases System Robustness with Added Manual Reset
- Precision Monitoring of 3V, 3.3V, and 5V Power-Supply Voltages
- 140ms Min Power-On-Reset Pulse Width-- RESET Output
- Guaranteed Over Temperature
- Power-Supply Transient Immunity

Saves Board Space
- No External Components
- 4-Pin SOT143 Package

Low Power Consumption Simplifies Power-Supply Requirements
- 6µA Supply Current

■ ORDERING INFORMATION

Part Number	Package	Packing	Temperature	Package Qty	V_{RT}
TK812MEUS	SOT-143-4	Reel	-40°C ~ 85°C (TA)	2500	4.38V
TK812SEUS	SOT-143-4	Reel	-40°C ~ 85°C (TA)	2500	2.93V
TK812LEUS	SOT-143-4	Reel	-40°C ~ 85°C (TA)	2500	4.63V
TK812REUS	SOT-143-4	Reel	-40°C ~ 85°C (TA)	2500	2.63V
TK812TEUS	SOT-143-4	Reel	-40°C ~ 85°C (TA)	2500	3.08V

■ APPLICATIONS

* Critical µP and µC Power Monitoring
* Portable/Battery-Powered Equipment
* Intelligent Instruments
* Controllers

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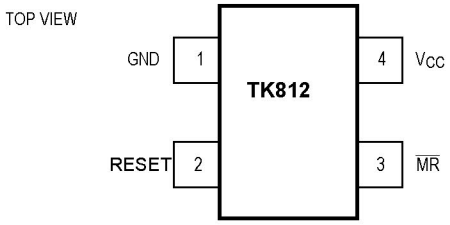
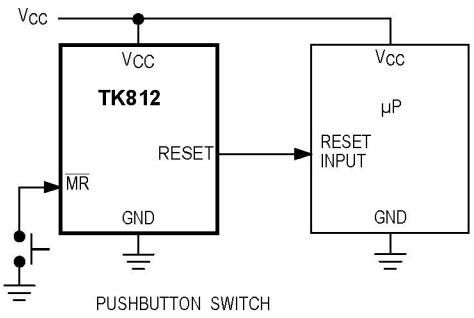
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN TK812	NAME	FUNCTION
1	GND	Ground
2	RESET	Active-High Reset Output. RESET remains high while V_{CC} is below the reset threshold or while $\overline{MR}$ is held low. RESET remains high for Reset Active Timeout Period (t_{RP}) after the reset conditions are terminated.
3	$\overline{MR}$	Manual Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted as long as $\overline{MR}$ is low and for 180ms after $\overline{MR}$ returns high. This active-low input has an internal 20kΩ pull-up resistor. It can be driven from a TTL or CMOS-logic line, or shorted to ground with a switch. Leave open if unused.
4	V_{CC}	+5V, +3.3V, or +3V Supply Voltage

■ BLOCK DIAGRAM



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■ ABSOLUTE MAXIMUM RATING

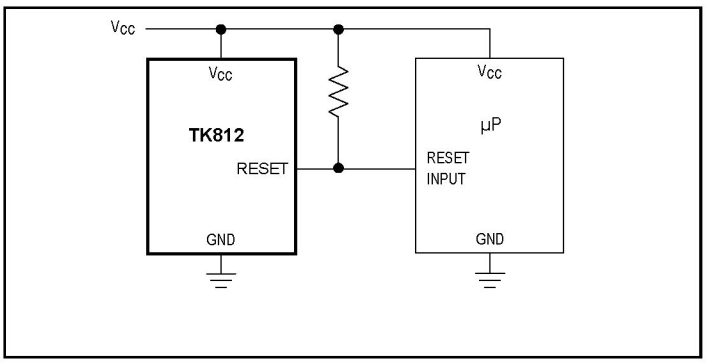
PARAMETER	SYMBOL	RATINGS	UNIT
Terminal Voltage (with respect to GND)	V_{CC}	-0.3 ~ 6.0	V
All Other Inputs		-0.3 ~ (V_{CC}+0.3V)	V
Input Current, V_{CC}, $\overline{MR}$	I_{CC}	20	mA
Output Current, (all outputs)	$\overline{RESET}$	20	mA
Junction Temperature	T_J	+150	℃
Operating Temperature Range	T_{OPR}	-40 ~ +85	℃
Storage Temperature	T_{STG}	-65 ~ +160	℃
Continuous Power Dissipation		320	mW

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_J, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{cc}		1.2		5.5	V
Supply Current	I_{cc}			6	15	μA
Reset Threshold	V_{TH}	TK81_L	4.54	4.63	4.72	V
Reset Threshold	V_{TH}	TK81_M	4.30	4.38	4.46	V
Reset Threshold	V_{TH}	TK81_T	3.03	3.08	3.14	V
Reset Threshold	V_{TH}	TK81_S	2.88	2.93	2.98	V
Reset Threshold	V_{TH}	TK81_R	2.58	2.63	2.68	V
Reset Threshold Tempco				30		ppm/°C
VCC to Reset Delay		V_{OD} = 125mV, TK81_L/M		40		μs
		V_{OD} = 125mV, TK81_R/S/T		20		
Reset Active Timeout Period	t_{RP}	V_{CC} = V_{TH} (max)	140	240	560	ms
$\overline{MR}$ Minimum Pulse Width	t_{MR}		10			μs
$\overline{MR}$ Glitch Immunity				100		ns
$\overline{MR}$ Pull-Up Resistance		V_{CC} = V_{TH} (max), I_{SINK} = 3.2mA,		0.5		μs
RESET Output Voltage	V_{OH}	TK812R/S/T only, I_{SINK} = 1.2mA, V_{CC} = V_{TH}(MAX)			0.3	V
		TK812L/M only, I_{SINK} = 3.2mA, V_{CC} = V_{TH}(MAX)			0.4	

■ TYPICAL APPLICATION CIRCUIT



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■ Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. These µP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

$\overline{RESET}$ is guaranteed to be a logic low for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period; after this interval, $\overline{RESET}$ goes high.

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{RESET}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{RESET}$ goes low. The internal timer starts after VCC returns above the reset threshold, and $\overline{RESET}$ remains low for the reset timeout period.

The manual reset input ($\overline{MR}$) can also initiate a reset. See the *Manual Reset Input* section.

The TK812 has an active-high RESET output that is the inverse of the TK811's $\overline{RESET}$ output.

Manual Reset Input

Many µP-based products require manual reset capabil-ity, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for the Reset Active Timeout Period (t_{RP}) after $\overline{MR}$ returns high. This input has an internal 20kΩ pull-up resistor, so it can be left open if it is not used. $\overline{MR}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity.

Reset Threshold Accuracy

The TK811/TK812 are ideal for systems using a 5V ±5% or 3V ±5% power supply with ICs specified for 5V ±10% or 3V ±10%, respectively. They are designed to meet worst-case specifications over temperature. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range for the system ICs. The thresholds are pre-trimmed and exhibit tight dis-tribution, reducing the range over which an undesirable reset may occur.

■ APPLICATIONS INFORMATION

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the TK811/TK812 are relatively immune to short duration negative-going VCC transients (glitches).

Figure 1 shows typical transient durations vs. reset com-parator overdrive, for which the TK811/TK812 do not generate a reset pulse. This graph was generated using a negative-going pulse applied to VCC, starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going VCC transient may have without causing a reset pulse to be issued. As the magnitude of the tran-sient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a VCC transient that goes 125mV below the reset thresh-old and lasts 40µs or less (TK81_L/M) or 20µs or less (TK81_T/S/R) will not cause a reset pulse to be issued.A 0.1µF capacitor mounted as close as possible to VCC provides additional transient immunity.

Ensuring a Valid Reset Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the TK811 $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS-logic inputs connected to the $\overline{RESET}$ output can drift to undetermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with VCC below 1V. However, in applications where the $\overline{RESET}$ output must be valid down to 0V, adding a pulldown resistor to the $\overline{RESET}$ pin will cause any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 2). R1's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

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A 100kΩ pull-up resistor to V_{CC} is also recommended for the TK812 if RESET is required to remain valid for VCC < 1V.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins (such as the Motorola 68HC11 series) can contend with the TK811/TK812 reset outputs. If, for example, the TK811 $\overline{\text{RESET}}$ output is asserted high and the µP wants to pull it low, indeter-minate logic levels may result. To correct such cases, connect a 4.7kΩ resistor between the TK811 $\overline{\text{RESET}}$ (or TK812 RESET) output and the µP reset I/O (Figure 3). Buffer the reset output to other system components.

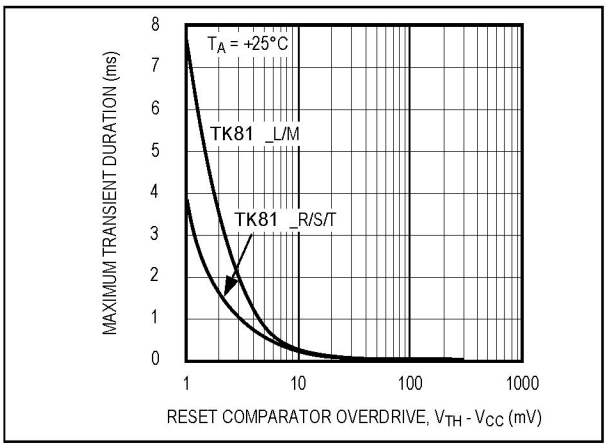

Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Comparator Overdrive

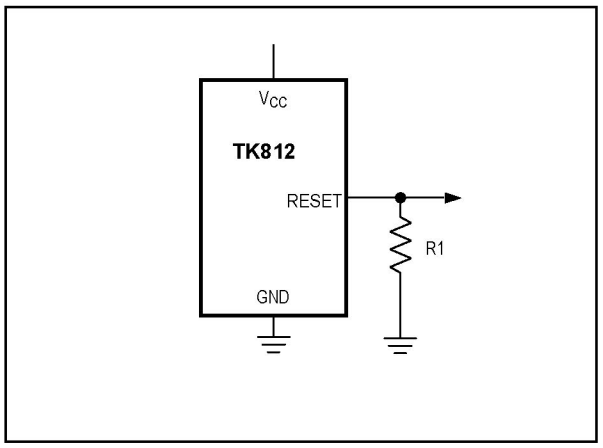

Figure 2. RESET Valid to V_{CC} = Ground Circuit

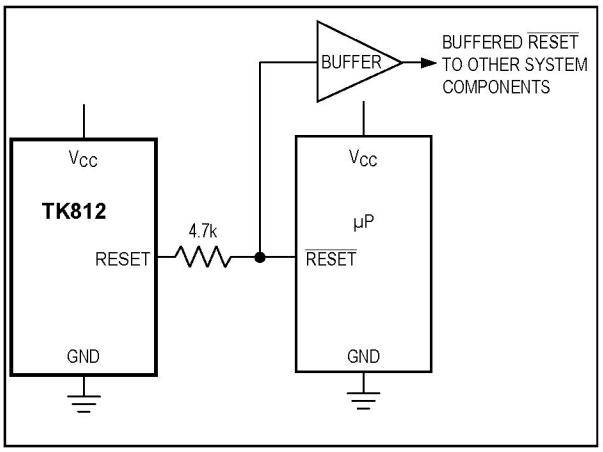

Figure 3. Interfacing to µPs with Bidirectional Reset I/O

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