LOW COST MICROPROCESSOR SUPERVISORY CIRCUITS

DESCRIPTION

The TK708 microprocessor supervisory circuit reduces the complexity and number of components required to monitor power-supply and monitor microprocessor activity. It significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The TK708 provides power-supply monitoring circuitry that generates a reset output during power-up, power-down and brownout conditions. The reset output remains operational with VCC as low as 1V.

In addition, there is a 1.25V threshold detector for power-fail warning, low-battery detection, or monitoring an additional power supply.

FEATURES

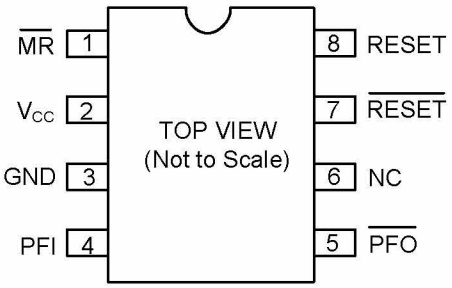
* Precision supply- Voltage Monitor
* Valid $\overline{\text{RESET}}$ remains with VCC as low as 1V
* 200ms Reset Pulse Width
* Voltage Monitor for Power-Fail or Low-Battery Warning
* With Manual reset input

SOIC - 8,
1.75 mm max height

ORDERING INFORMATION

Part Number	Package	Packing	Temperature(TA)	Package Qty	V_{RT}
TK708CSA	SOIC-8	Reel	0°C ~ 70°C	2500	4.4V
TK708ESA	SOIC-8	Reel	-40°C ~ 85°C	2500	4.4V
TK708RCSA	SOIC-8	Reel	0°C ~ 70°C	2500	2.63V
TK708RESA	SOIC-8	Reel	-40°C ~ 85°C	2500	2.63V
TK708SCSA	SOIC-8	Reel	0°C ~ 70°C	2500	2.93V
TK708SESA	SOIC-8	Reel	-40°C ~ 85°C	2500	2.93V
TK708TCSA	SOIC-8	Reel	0°C ~ 70°C	2500	3.08V
TK708TESA	SOIC-8	Reel	-40°C ~ 85°C	2500	3.08V

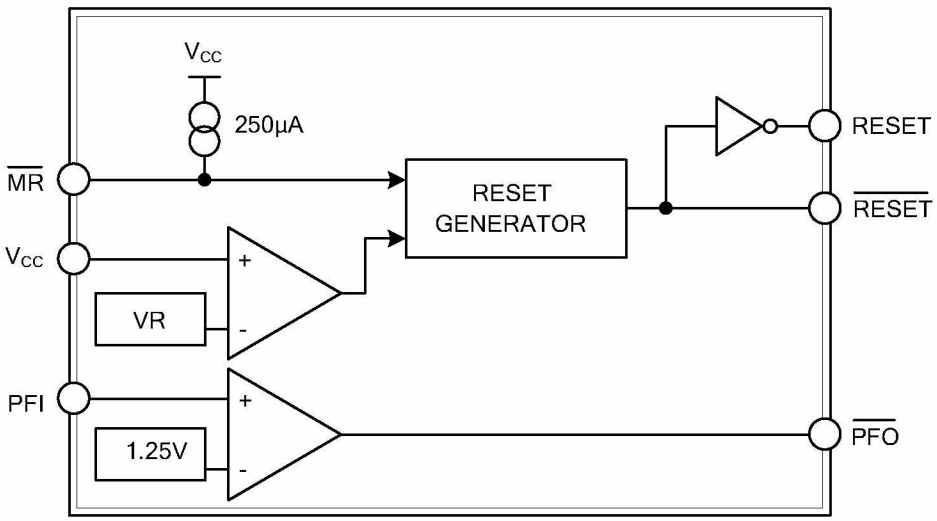
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{MR}$	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 500μA (V_{CC}=+5V) pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	V_{CC}	Power Supply Voltage that is monitored.
3	GND	0V Ground Reference for all signals.
4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
6	NC	NC
7	$\overline{RESET}$	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold. It remains low for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high.
8	RESET	Logic Output. RESET is an active high output suitable for systems that use active high reset logic. It is the inverse of $\overline{RESET}$.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

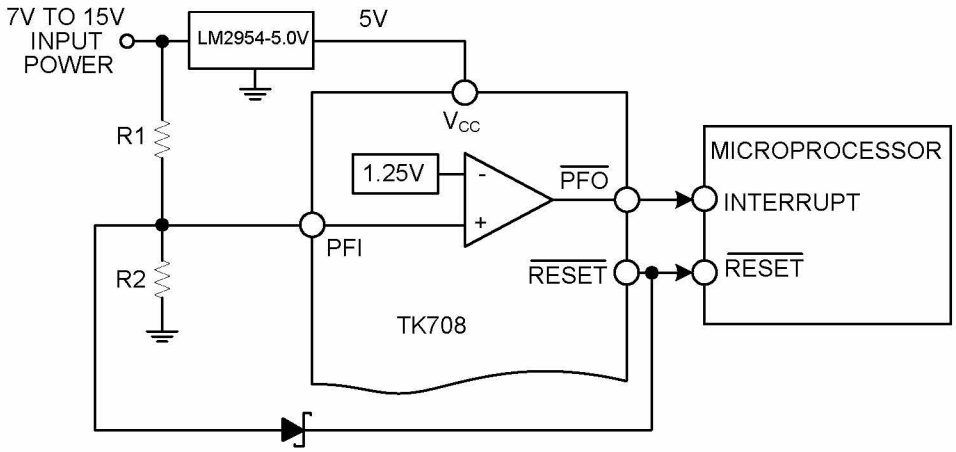
PARAMETER	SYMBOL	RATINGS	UNIT
Terminal Voltage (with respect to GND)	V_{CC}	-0.3 ~ 6.0	V
All Other Inputs	V_{IN}	-0.3 ~ (V_{CC}+0.3V)	V
Input Current, V_{CC}, GND	I_{CC}	20	mA
Output Current, (all outputs)	I_{OUT}	20	mA
Junction Temperature	T_J	+150	℃
Operating Temperature Range	T_{OPR}	C:0 ~ +70 E:-40 ~ +85	℃
Storage Temperature	T_{STG}	-65 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_J, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		V_{CC}		1.0		5.5	V
Supply Current		I_{SUPPLY}			50	150	μA
Reset Threshold				4.25	4.40	4.45	V
Reset Threshold Hysteresis					60		mV
Reset Pulse Width		t_{RS}		120	200	280	ms
$\overline{RESET}$ 、RESET Output Voltage			I_{SOURCE} =800μA	V_{CC}-1.5			V
			I_{sink}=3.2mA			0.4	V
			V_{CC}=1V, I_{sink}=50μA			0.3	V
$\overline{MR}$ Pull-Up Current			$\overline{MR}$ = 0V		500		μA
$\overline{MR}$ Pulse Width		t_{MR}		250			ns
$\overline{MR}$ Input Threshold	Low		T_A = +25°C			0.8	V
	High			2			V
$\overline{MR}$ to Reset Out Delay		t_{MD}				350	ns
PFI Input Threshold				1.18	1.25	1.3	V
PFI Input Current			V_{CC}= 5V		0.2		nA
$\overline{PFO}$ Output Voltage			I_{SOURCE}=800μA	V_{CC}-1.5			V
			I_{sink}=3.2mA			0.4	V

■ TYPICAL APPLICATION CIRCUIT



Applications Information

Ensuring a Valid RESET Output Down to VCC = 0V

When V_{CC} falls below 1V, the TK705–TK708 $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pulldown resistor is added to the $\overline{RESET}$ pin, as shown in Figure 5, any stray charge or leakage currents will be drained to ground, holding $\overline{RESET}$ low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load $\overline{RESET}$ and small enough to pull RESET to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage-divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND reduces the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{RESET}$ can be asserted on

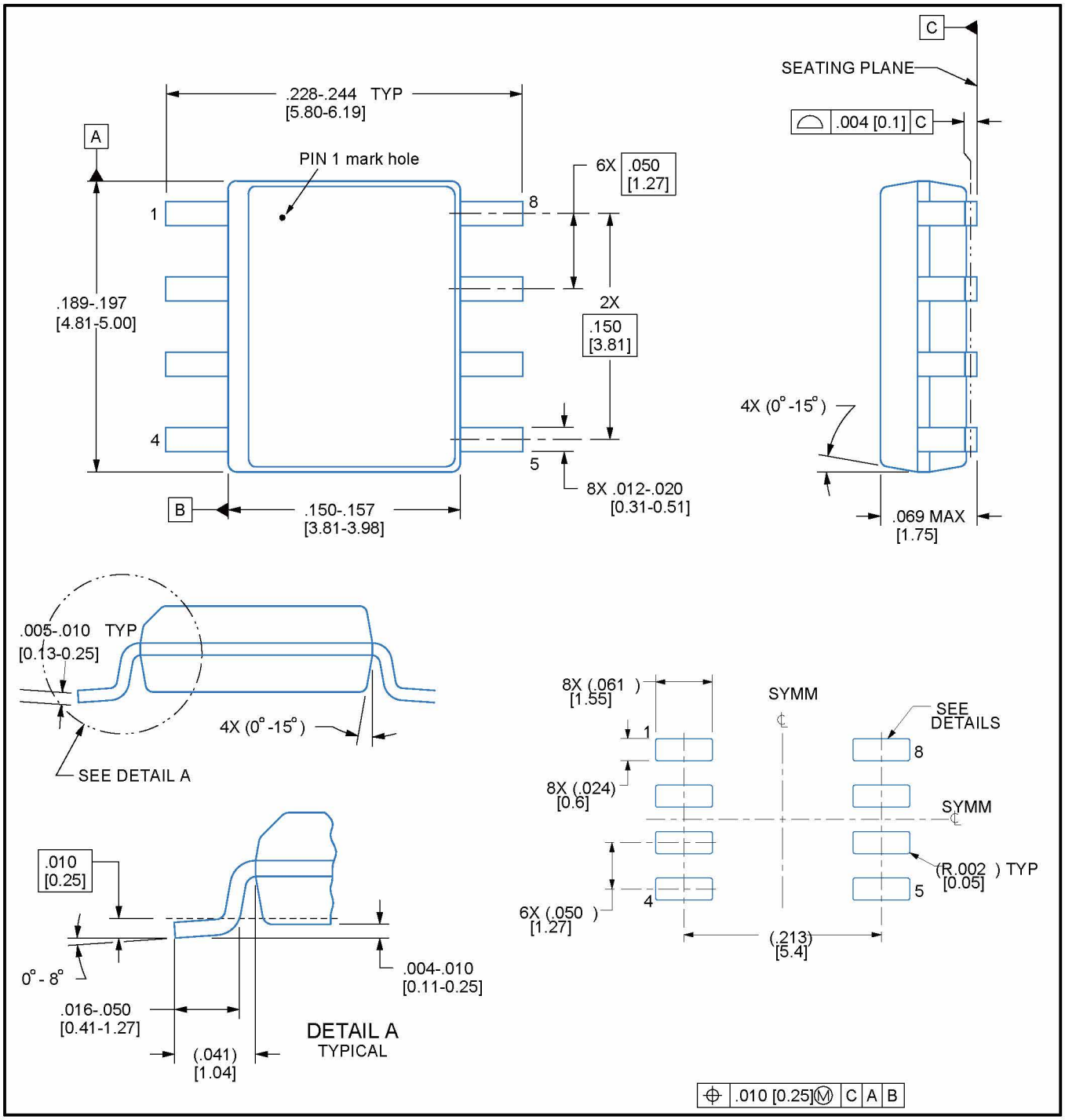
other voltages in addition to the +5V V_{CC} line. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a $\overline{RESET}$ pulse when PFI drops below 1.25V. Figure 6 shows the TK708 con igured to assert $\overline{RESET}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 7). When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{PFO}$ is high. By adding the resistors and transistor as shown, a high $\overline{PFO}$ triggers a reset. As long as $\overline{PFO}$ remains high, the TK705–TK708/TK813L keep reset asserted ($\overline{RESET}$ = low, RESET = high). Note that this circuit's accuracy depends on the PFI

threshold tolerance, the V_{CC} line, and the resistors.

PACKAGE OUTLINE SOIC - 8,1.75 mm max height



NOTES: Linear dimensions are in inches [millimeters]. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.