LOW COST MICROPROCESSOR SUPERVISOR CIRCUITS

■ DESCRIPTION

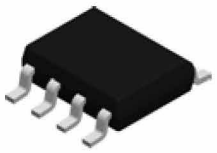
The TK706 microprocessor supervisory circuit reduces the complexity and number of components required to monitor power-supply and monitor microprocessor activity. It significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The TK706 provides power-supply monitoring circuitry that generates a reset output during power-up, power-down and brownout conditions. The reset output remains operational with VCC as low as 1V.

In addition, there is a 1.25V threshold detector for power-fail warning, low-battery detection, or monitoring an additional power supply.

■ FEATURES

* Precision supply- Voltage Monitor
* Valid $\overline{\text{RESET}}$ remains with V_{CC} as low as 1V
* 200ms Reset Pulse Width
* Voltage Monitor for Power-Fail or Low-Battery Warning
* With Manual reset input

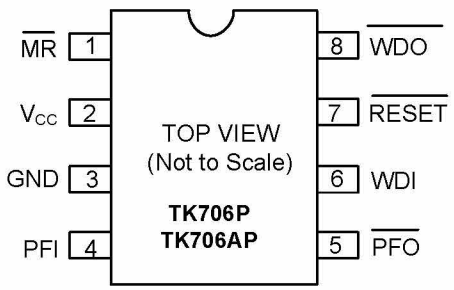


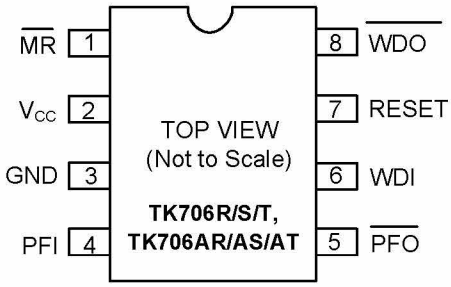
SOIC - 8,
1.75 mm max height

■ ORDERING INFORMATION

Part Number	Package	Packing	Temperature(TA)	Package Qty	V_{RT}
TK706CSA	SOIC-8	Reel	0°C ~ 70°C	2500	4.4V
TK706ESA	SOIC-8	Reel	-40°C ~ 85°C	2500	4.4V
TK706TCSA	SOIC-8	Reel	0°C ~ 70°C	2500	3.08V
TK706TESA	SOIC-8	Reel	-40°C ~ 85°C	2500	3.08V
TK706RCSA	SOIC-8	Reel	0°C ~ 70°C	2500	2.63V
TK706RESA	SOIC-8	Reel	-40°C ~ 85°C	2500	2.63V
TK706PCSA	SOIC-8	Reel	0°C ~ 70°C	2500	2.63V
TK706PESA	SOIC-8	Reel	-40°C ~ 85°C	2500	2.63V
TK706ARESA	SOIC-8	Reel	-40°C ~ 85°C	2500	2.63V
TK706SCSA	SOIC-8	Reel	0°C ~ 70°C	2500	2.93V
TK706SESA	SOIC-8	Reel	-40°C ~ 85°C	2500	2.93V
TK706ASESA	SOIC-8	Reel	-40°C ~ 85°C	2500	2.93V

■ PIN CONFIGURATION





■ PIN DESCRIPTION

TK706P TK706AP SOIC8	TK706R/S/T, TK706AR/AS/AT SOIC8	NAME	FUNCTION
1	1	MR	Active-Low, Manual-Reset Input. Pull MR below 0.6V to trigger a r eset pulse. MR is TTL/CMOS compatible when V_{CC} = 5V and can be shorted to GND with a switch. MR is internally connected to a 70μA source current. Connect to V_{CC} or leave unconnected.
2	2	V_{CC}	Supply Voltage Input
3	3	GND	Ground
4	4	PFI	Adjustable Power-Fail Comparator Input. Connect PFI to a resistive divider to set the desired PFI threshold. When PFI is less than 1.25V, PFO goes low and sinks current; otherwise, PFO remains high. Connect PFI to GND if not used.
5	5	PFO	Active-Low, Power-Fail Comparator Output. PFO asserts when PFI is below the internal 1.25V threshold. PFO deasserts when PFI is above the internal 1.25V threshold. Leave PFO unconnected if not used.
6	6	WDI	Watchdog Input. A falling or rising transition must occur at WDI within 1.6s to prevent WDO from asserting (see Figure 4). The internal watchdog timer is reset to zero when reset is asserted or when transition occurs at WDI. The watchdog function for the TK706P/R/S/T can not be disabled. The watchdog timer for the TK706AP/AR/AS/AT disables when WDI input is left open or connected to a tri-state output in its high-impedance state with a leakage current of less than 600nA.
7	—	RESET	Active-High Reset Output. RESET remains high when V_{CC} is below the reset threshold or MR is held low. It remains low for 200ms after the reset conditions end (Figure 3).
8	8	WDO	Active-Low Watchdog Output. WDO goes low when a transition does not occur at WDI within 1.6s and remains low until a transition occurs at WDI (indicating the watchdog interrupt has been serviced). WDO also goes low when V_{CC} falls below the reset threshold; however, unlike the reset output signal, WDO goes high as soon as V_{CC} rises above the reset threshold.
—	7	RESET	Active-Low Reset Output. RESET remains low when V_{CC} is below the reset threshold or MR is held low. It remains low for 200ms after the reset conditions end (Figure 3).

■ ELECTRICAL CHARACTERISTICS (T_J, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}		TK70_C	1.0		5.5	V
			TK70_E/M	1.2		5.5	
Supply Current	I_{SUPPLY}	V_{CC} < 3.6V	TK706_C		90	200	µA
			TK706_E/M		90	300	
		V_{CC} < 5.5V	TK706_C		135	350	
			TK706_E/M		135	500	
Reset Threshold (Note 3)(V_{CC} Falling)	V_{RST}	TK70_P/R, TK706AP/AR		2.55	2.63	2.70	V
		TK70_S, TK706AS		2.85	2.93	3.00	
		TK70_T, TK706AT		3.00	3.08	3.15	
Reset Threshold Hysteresis (Note 3)	V_{HYS}				20		mV
Reset Pulse Width (Note 3)	t_{RST}	TK70_P/R, TK706AP/AR V_{CC} = 3.0V		140	200	280	ms
		TK70_S, TK706AS, V_{CC} = 3.3V		140	200	280	
		V_{CC} = 5V			200		
RESET OUTPUT							
Output-Voltage High (TK70_R/S/T) (TK706AR/AS/AT)	V_{OH}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	$I_{RSOURCE}$ = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V	I_{SINK} = 3.2mA			0.4	
	V_{OL}	TK70_C V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		TK70_E/M: VCC = 1.2V, ISINK = 100µA				0.3	
Output-Voltage High (MAX706P) (MAX706AP)	V_{OH}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SOURCE} = 215µA	V_{CC} – 0.6			V
	V_{OL}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5 < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V	I_{SINK} = 3.2mA			0.4	
WATCHDOG INPUT							
Watchdog Timeout Period	t_{WD}	TK706P/R,TK706AP/AR, V_{CC} = 3.0V		1.00	1.6	2.25	s
		TK706S/T, TK706AS/AT, V_{CC} = 3.3V		1.00	1.6	2.25	
WDI Pulse Width (TK706_, TK706A_)	t_{WP}	V_{IL} = 0.4V	$V_{RST(MAX)}$ < V_{CC} < 3.6V	100			ns
		V_{IH} = 0.8V x V_{CC}	4.5V < V_{CC} < 5.5V	50			
Watchdog Input Threshold (TK706_, TK706A_)	V_{IL}	$V_{RST(MAX)}$ < V_{CC} < 3.6V				0.6	V
	V_{IH}	$V_{RST(MAX)}$ < V_{CC} < 3.6V		0.7 x V_{CC}			
	V_{IL}	V_{CC} = 5.0V				0.8	
	V_{IH}	V_{CC} = 5.0V		3.5			
WDI Input Current		WDI = 0V or V_{CC}	TK706_	-1.0	+0.02	+1.0	µA
			TK706A_	-5		+5	

ELECTRICAL CHARACTERISTICS (continued)

(TK70_P/R, TK706AP/AR: V_{CC} = 2.7V to 5.5V; TK70_S, TK706AS: V_{CC} = 3.0V to 5.5V; TK70_T, TK706AT: V_{CC} = 3.15V to 5.5V; T_J = T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_J = T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
WATCHDOG OUTPUT							
WDO Output Voltage (TK706_, TK706A_)	V_{OH}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SINK} = 500µA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V	I_{SINK} = 1.2mA			0.4	
MANUAL RESET INPUT							
MR Pullup Current		MR = 0	$V_{RST(MAX)}$ < V_{CC} < 3.6V	25	70	250	µA
			4.5V < V_{CC} < 5.5V	100	250	600	
MR Pulse Width	t_{MR}	$V_{RST(MAX)}$ < V_{CC} < 3.6V		500			ns
		4.5V < V_{CC} < 5.5V		150			
MR Input Threshold	V_{IL}	$V_{RST(MAX)}$ < V_{CC} < 3.6V				0.6	V
	V_{IH}	$V_{RST(MAX)}$ < V_{CC} < 3.6V		0.7 x V_{CC}			
	V_{IL}	4.5V < V_{CC} < 5.5V				0.8	
	V_{IH}	4.5V < V_{CC} < 5.5V		2.0			
MR to Reset Output Delay	t_{MD}	$V_{RST(MAX)}$ < V_{CC} < 3.6V				750	ns
		4.5V < V_{CC} < 5.5V				250	
POWER-FAILURE COMPARATOR							
PFI Input Threshold		(TK70_P/R, TK706AP/AR) PFI falling V_{CC} = 3.0V		1.2	1.25	1.3	V
		(TK70_S/T, TK706AS/AT) PFI falling, V_{CC} = 3.3V		1.2	1.25	1.3	
PFI Input Current				-25	+0.01	+25	nA
PFO Output Voltage	V_{OH}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V	I_{SINK} = 3.2mA			0.4	

Note 2: All devices 100% production tested at T_A = +85°C. Limits over temperature are guaranteed by design.

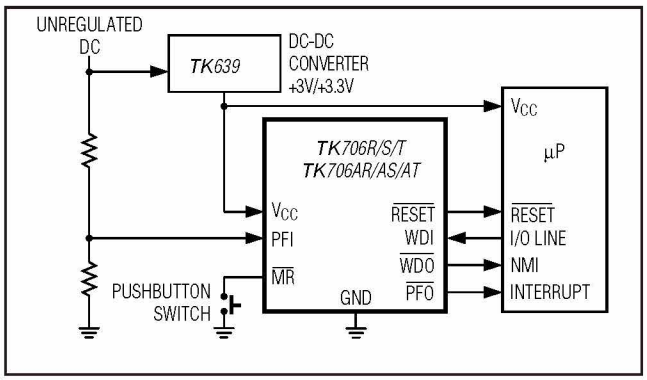
Note 3: Applies to both RESET in the TK70_R/S/T and TK706AR/AS/AT, and RESET in the TK706P/TK706AP.

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Terminal Voltage (with respect to GND)	V_{CC}	-0.3 ~ 6.0	V
All Other Inputs	V_{IN}	-0.3 ~ (V_{CC}+0.3V)	V
Input Current, V_{CC}, GND	I_{CC}	20	mA
Output Current, (all outputs)	I_{OUT}	20	mA
Junction Temperature	T_J	+150	℃
Operating Temperature Range	T_{OPR}	C:0 ~ +70 E:-40 ~ +85	℃
Storage Temperature	T_{STG}	-65 ~ +150	℃
8-Pin SO (derate 5.9mW/°C above +70°C).		470	mW

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ TYPICAL APPLICATION CIRCUIT



Typical Operating Circuits continued at end of data sheet.

Applications Information

Ensuring a Valid RESET Output Down to CC 0

When V_{CC} falls below 1V, the TK705–TK708 $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pulldown resistor is added to the $\overline{\text{RESET}}$ pin, as shown in Figure 5, any stray charge or leakage currents will be drained to ground, holding $\overline{\text{RESET}}$ low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load $\overline{\text{RESET}}$ and small enough to pull RESET to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage-divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{\text{PFO}}$. A capacitor between PFI and GND reduces the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{\text{RESET}}$ can be asserted on

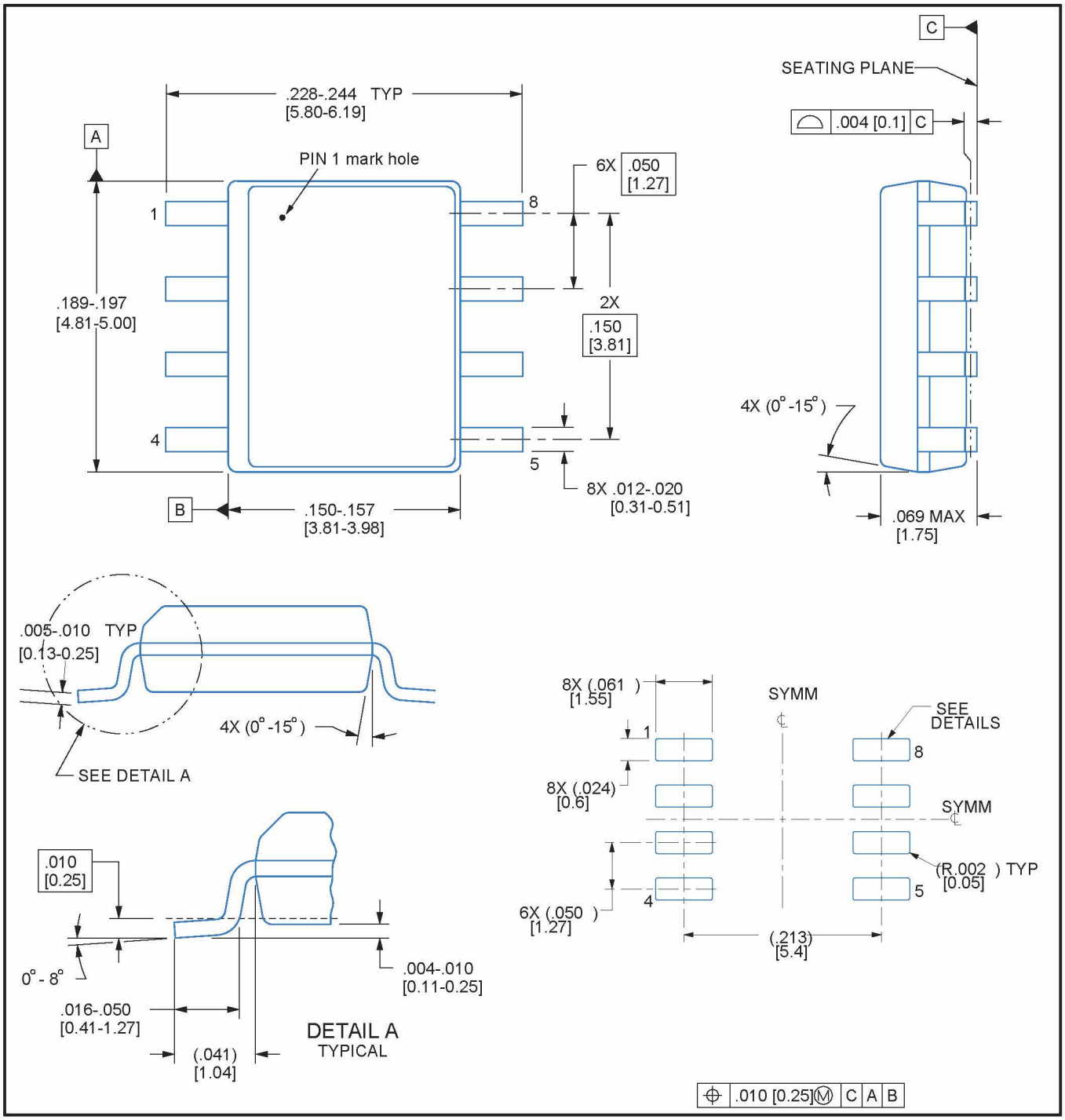
other voltages in addition to the +5V V_{CC} line. Connect $\overline{\text{PFO}}$ to $\overline{\text{MR}}$ to initiate a $\overline{\text{RESET}}$ pulse when PFI drops below 1.25V. Figure 6 shows the TK706 con igured to assert $\overline{\text{RESET}}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 7). When the negative rail is good (a negative voltage of large magnitude), $\overline{\text{PFO}}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{\text{PFO}}$ is high. By adding the resistors and transistor as shown, a high $\overline{\text{PFO}}$ triggers a reset. As long as $\overline{\text{PFO}}$ remains high, the TK705–TK708/ TK813L keep reset asserted ($\overline{\text{RESET}}$ = low, RESET = high). Note that this circuit's accuracy depends on the PFI

threshold tolerance, the V_{CC} line, and the resistors.

PACKAGE OUTLINE SOIC - 8,1.75 mm max height



NOTES: Linear dimensions are in inches [millimeters]. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.