LOW COST MICROPROCESSOR SUPERVISOR CIRCUITS

■ DESCRIPTION

The TK705 microprocessor supervisory circuit reduces the complexity and number of components required to monitor power-supply and monitor microprocessor activity. It significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The TK705 provides power-supply monitoring circuitry that generates a reset output during power-up, power-down and brownout conditions. The reset output remains operational with VCC as low as 1V.

In addition, there is a 1.25V threshold detector for power-fail warning, low-battery detection, or monitoring an additional power supply.

■ FEATURES

Precision supply- Voltage Monitor

Valid $\overline{\text{RESET}}$ remains with V_{CC} as low as 1V

200ms Reset Pulse Width

Voltage Monitor for Power-Fail or Low-Battery Warning

With Manual reset input

Precision-Supply Voltage Monitor - 4.65V

SOIC - 8,
1.75 mm max height

■ APPLICATIONS

Computers

Controllers

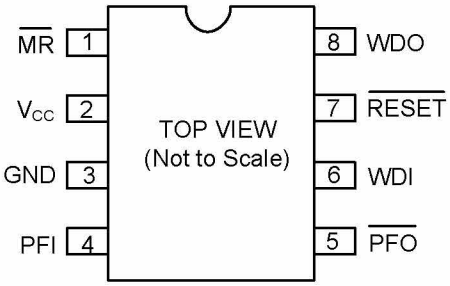
Intelligent Instruments

Critical µP Power Monitoring

■ ORDERING INFORMATION

Part Number	Package	Packing	Temperature	Package Qty	V_{RT}
TK705CSA	SOIC-8	Reel	0°C ~ 70°C（TA）	2500	4.65V
TK705ESA	SOIC-8	Reel	-40°C ~ 85°C（TA）	2500	4.65V

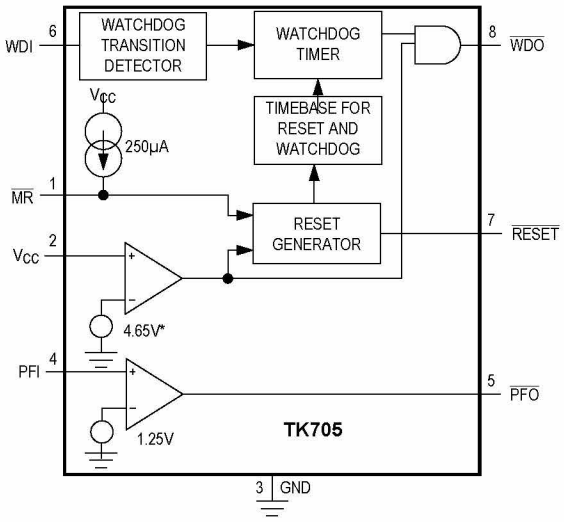
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{MR}$	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 500μA (V_{CC}=+5V) pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	V_{CC}	Power Supply Voltage that is monitored.
3	GND	0V Ground Reference for all signals.
4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V otherwise $\overline{PFO}$ stays high.
6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and WDO goes low (Figure 1). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three stated, or WDI sees a rising or falling edge.
7	$\overline{RESET}$	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold. It remains low for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high.
8	$\overline{WDO}$	Watchdog Output pulls low when the internal watchdog timer inishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

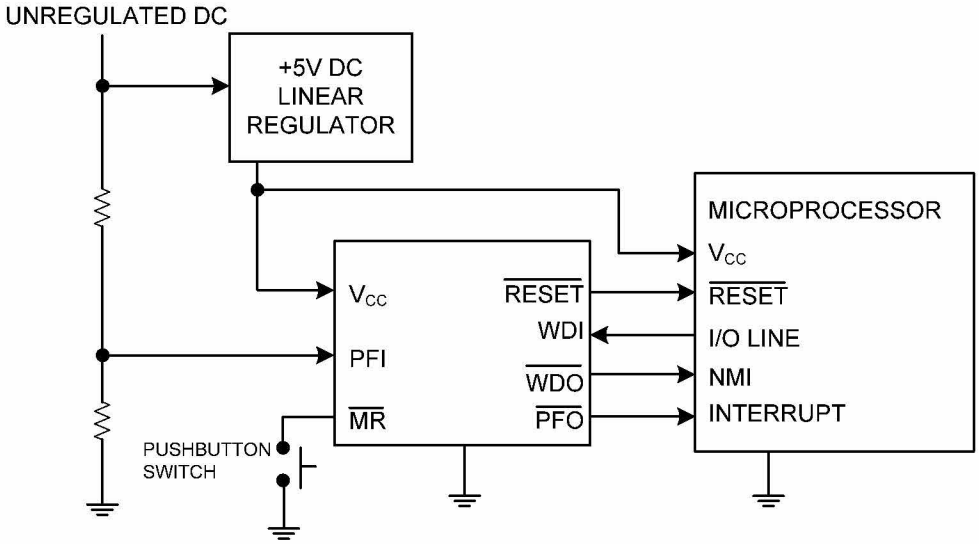
PARAMETER	SYMBOL	RATINGS	UNIT
Terminal Voltage (with respect to GND)	V_{CC}	-0.3 6.0	V
All Other Inputs	V_{IN}	-0.3 (V_{CC}+0.3V)	V
Input Current, V_{CC}, GND	I_{CC}	20	mA
Output Current, (all outputs)	I_{OUT}	20	mA
unction Temperature	T	+150	C
Operating Temperature Range	T_{OPR}	C:0 +70 E:-40 +85	C
Storage Temperature	T_{STG}	-65 +150	C
SOIC(derate 5.88mW/ C above +70 C)		471	mW

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		V_{CC}		1.0		5.5	V
Supply Current		I_{SUPPLY}			150	350	µA
Reset Threshold				4.5	4.65	4.75	V
Reset Threshold Hysteresis					40		mV
Reset Pulse Width		t_{RS}		140	200	280	ms
$\overline{\text{RESET}}$ Output Voltage			I_{SOURCE} =800µA	V_{CC}-1.5			V
			I_{sink}=3.2mA			0.4	V
			V_{CC}=1V, I_{sink}=50µA			0.3	V
$\overline{\text{MR}}$ Pull-Up Current			$\overline{\text{MR}}$ = 0V		500		µA
$\overline{\text{MR}}$ Pulse Width		t_{MR}		250			ns
$\overline{\text{MR}}$ Input Threshold	Low		T_A = +25°C			0.8	V
	High			2			V
$\overline{\text{MR}}$ to Reset Out Delay		t_{MD}				350	ns
PFI Input Threshold				1.18	1.25	1.3	V
PFI Input Current			V_{CC}= 5V		0.2		nA
$\overline{\text{PFO}}$ Output Voltage			I_{SOURCE}=800µA	V_{CC}-1.5			V
			I_{sink}=3.2mA			0.4	V
		t_{WD}		1.00	1.60	2.25	s
WDI Pulse Width		t_{WP}	V_{IL} = 0.4V, V_{IH} = (V_{CC}) (0.8)	50			ns
WDI Input Threshold	Low		V_{CC} = 5V			0.8	V
	High			3.5			
WDI Input Current			V_{CC} = 5V		50	150	µA
			WDI = 0V	-150	-50		
$\overline{\text{WDO}}$ Output Voltage			I_{SOURCE} = 800µA	V_{CC} - 1.5			V
			I_{SINK} = 1.2mA			0.4	

■ TYPICAL APPLICATION CIRCUIT



Applications Information

Ensuring a Valid RESET Output Down to VCC 0V

When V_{CC} falls below 1V, the TK705 $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pulldown resistor is added to the $\overline{RESET}$ pin, as shown in Figure 1, any stray charge or leakage currents will be drained to ground, holding $\overline{RESET}$ low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load $\overline{RESET}$ and small enough to pull RESET to ground.

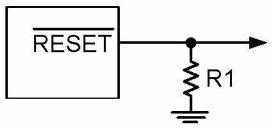


Figure 1. $\overline{RESET}$ Valid to Ground Circuit

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage-divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND reduces the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{RESET}$ can be asserted on

other voltages in addition to the +5V V_{CC} line. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a $\overline{RESET}$ pulse when PFI drops below 1.25V. Figure 6 shows the TK705 con.igured to assert $\overline{RESET}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

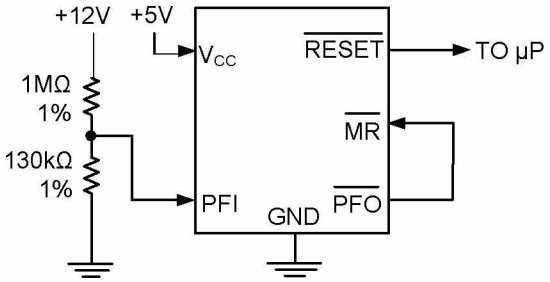
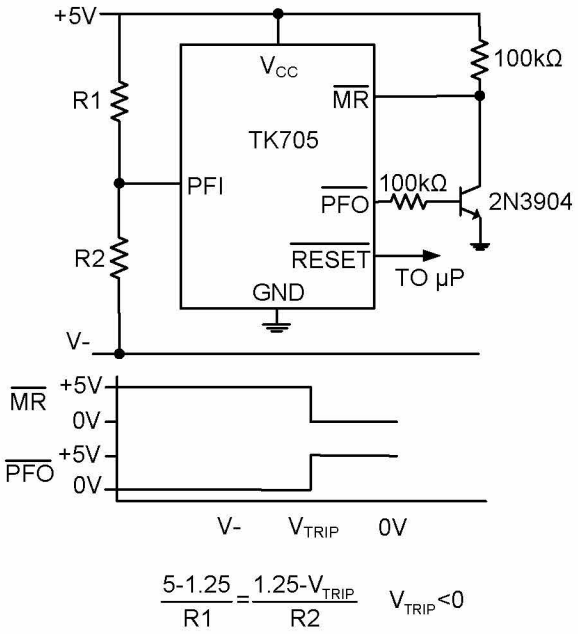


Figure 2.Monitoring Both +5V and +12V

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 3). When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{PFO}$ is high. By adding the resistors and transistor as shown, a high $\overline{PFO}$ triggers reset. As long as $\overline{PFO}$ remains high, the **TK705** will keep reset asserted ($\overline{RESET}$ = low, $\overline{RESET}$ = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.



$$\frac{5-1.25}{R1}=\frac{1.25-V_{TRIP}}{R2} \qquad V_{TRIP}<0$$

Figure 3.Monitoring a Negative Voltage

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins can contend with the **TK705** $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the Microprocessor wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as in Figure 4. Buffer the $\overline{RESET}$ output to other system components.

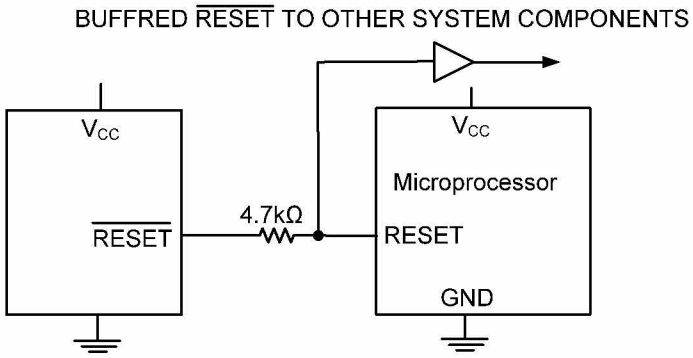
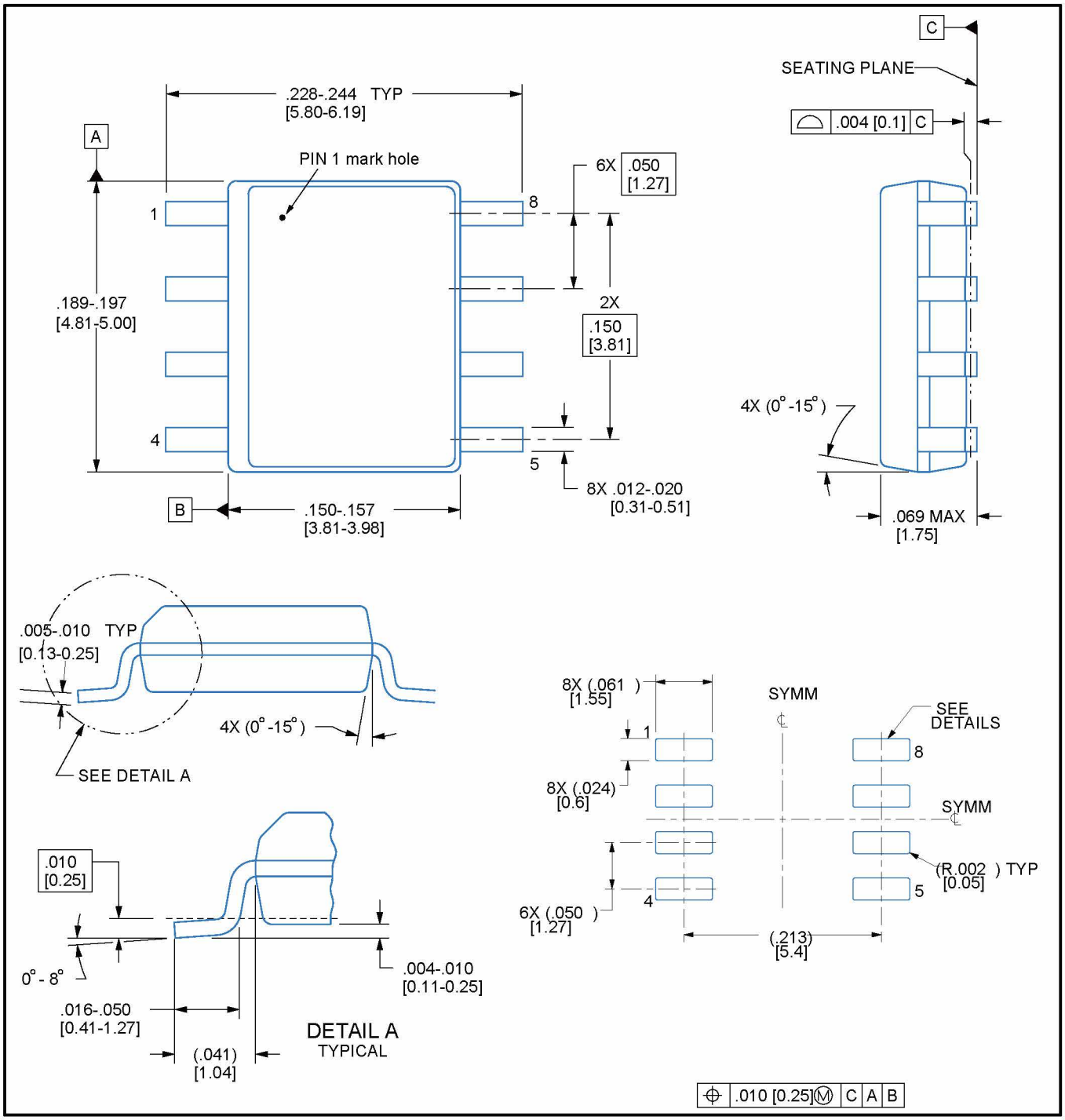


Figure . Interfacing to Microprocessors with Bidirectional Reset I

PACKAGE OUTLINE SOIC - 8,1.75 mm max height



NOTES: Linear dimensions are in inches [millimeters]. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.