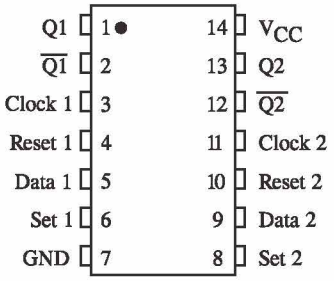
CMOS Dual D Flip-Flop

■ DESCRIPTION

The TK4013 is D type Flip-Flop,it consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, The TK4013 can connecting Q output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. The TK4013 can respective accomplishe a high level on the set or reset line.

■ PIN ASSIGNMENT



■ FEATURES

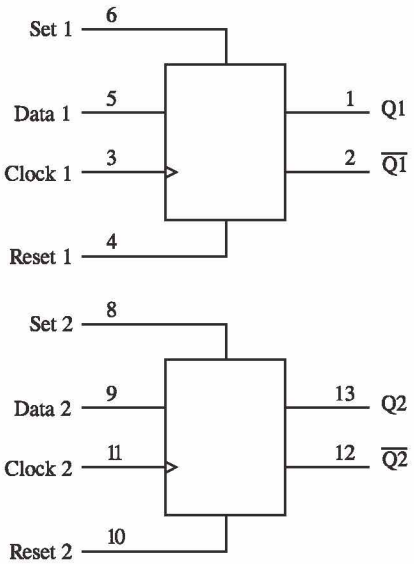
- Operating Voltage Range: 3 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5 V supply
  2.0 V min @ 10V supply
  2.5 V min @ 15 V supply
- Setting or resetting is independent of the clock
- TA = -40° to 125° C for all packages

■ FUNCTION TABLE

Inputs				Outputs	
Clock	Data	Reset	Set	Q	$\overline{Q}$
⌐‾	L	L	L	L	H
⌐‾	H	L	L	H	L
‾⌐	X	L	L	Q	$\overline{Q}$
X	X	H	L	L	H
X	X	L	H	H	L
X	X	H	H	H	H

X = don't care

■ LOGIC DIAGRAM



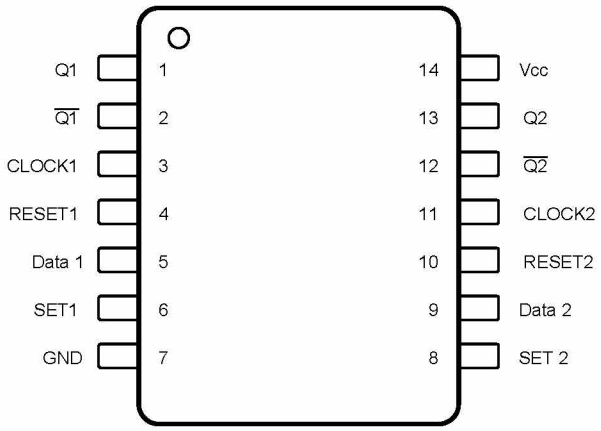
PIN 14 =V_{CC} PIN 7 = GND

■ Ordering information

Part Number	Package	Packing	Operating Temperature	Standard Package
TK4013BM	SOIC-14	Reel	-40°C ~ 125°C	2500
TK4013BP	TSSOP-14	Reel	-40°C ~ 125°C	2500
TK4013BE	DIP-14	Tube	-40°C ~ 125°C	1000

■ Pin Configuration and Functions

Top View



■ Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Q1	O	Channel 1 output
2	$\overline{Q1}$	O	Inverted channel 1 output
3	CLOCK1	I	Channel 1 clock input
4	RESET1	I	Channel 1 reset
5	Data 1	I	Channel 1 data input
6	SET1	I	Channel 1 set
7	GND	—	Ground
8	SET2	I	Channel 2 set
9	Data 2	I	Channel 2 data input
10	RESET2	I	Channel 2 reset
11	CLOCK2	I	Channel 2 clock input
12	$\overline{Q2}$	O	Inverted channel 2 output
13	Q2	O	Channel 2 output
14	V_{cc}	—	Power supply

■ MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Plastic DIP, SOIC Package	500	mW
P_{tot}	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-55 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Temperature.

■ RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}	DC Input Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation V_{IN} should be constrained to the range GND≤V_{IN} ≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

■ DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥ -55°C	25°C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V	5.0	3.5	3.5	3.5	V
		V_{OUT}=1.0 V or V_{CC} - 1.0 V	10	7	7	7	
		V_{OUT}=1.5 V or V_{CC} - 1.5 V	15	11	11	11	
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V	5.0	1.5	1.5	1.5	V
		V_{OUT}=1.0 V or V_{CC} - 1.0 V	10	3	3	3	
		V_{OUT}=1.5 V or V_{CC} - 1.5 V	15	4	4	4	
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
		V_{IL}=1.5V, V_{IH}=3.5V, I_O=-1μA	5.0	4.5	4.5	4.5	
		V_{IL}=3.0V, V_{IH}=7.0V, I_O=-1μA	10	9.0	9.0	9.0	
		V_{IL}=4.0V, V_{IH}=11V, I_O=-1μA	15	13.5	13.5	13.5	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
		V_{IL}=1.5V, V_{IH}=3.5V, I_O=1μA	5.0	0.5	0.5	0.5	
		V_{IL}=3.0V, V_{IH}=7.0V, I_O=1μA	10	1.0	1.0	1.0	
		V_{IL}=4.0V, V_{IH}=11V, I_O=1μA	15	1.5	1.5	1.5	
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC}					mA
		U_{OL}=0.4 V	5.0	0.64	0.51	0.36	
		U_{OL}=0.5 V	10	1.6	1.3	0.9	
		U_{OL}=1.5 V	15	4.2	3.4	2.4	
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC}					mA
		U_{OH}=2.5 V	5.0	-2.0	-1.6	-1.15	
		U_{OH}=4.6 V	5.0	-0.64	-0.51	-0.36	
		U_{OH}=9.5 V	10	-1.6	-1.3	-0.9	
		U_{OH}=13.5 V	15	-4.2	-3.4	-2.4	

■ AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55° C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
f_{max}	Maximum Clock Frequency (Figure 1)	5.0 10 15	3.5 8 12	3.5 8 12	3.0 6 10	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock Q or $\overline{Q}$ (Figure 1)	5.0 10 15	300 130 90	300 130 90	450 200 150	ns
t_{PLH}	Maximum Propagation Delay, Set to Q or Reset to $\overline{Q}$ (Figure 2)	5.0 10 15	300 130 90	300 130 90	450 200 150	ns
t_{PHL}	Maximum Propagation Delay, Set $\overline{Q}$ or Reset to Q (Figure 2)	5.0 10 15	400 170 120	400 170 120	600 250 150	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	250 150 100	ns
C_{IN}	Maximum Input Capacitance	5.0		7.5		pF

■ TIMING REQUIREMENTS(C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55° C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	140 60 40	140 60 40	200 80 50	ns
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	5.0 10 15	180 80 50	180 80 50	250 120 80	ns
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	5.0 10 15	40 20 15	40 20 15	40 20 15	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	5.0 10 15	5 5 5	5 5 5	8 5 5	ns
t_r, t_f	Maximum Input Rise or Fall Time, Clock (Figure 1)	5.0 10 15	500 30 6	500 30 6	500 30 6	μs

■ Switching Waveform

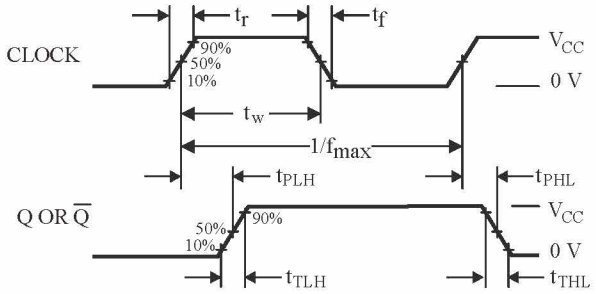


Figure 1. Switching Waveforms

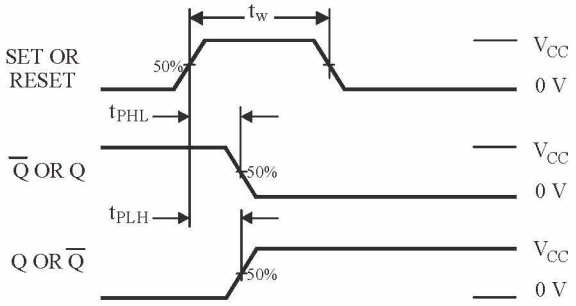


Figure 2. Switching Waveforms

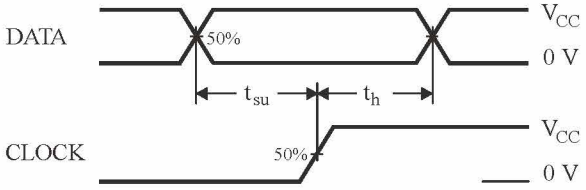
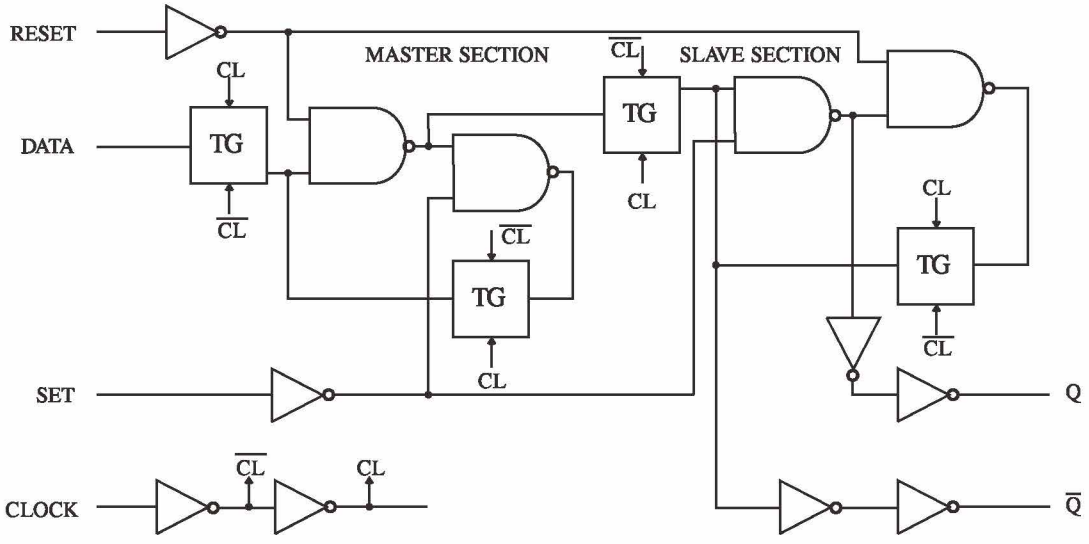
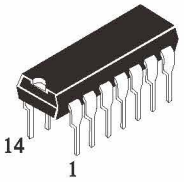


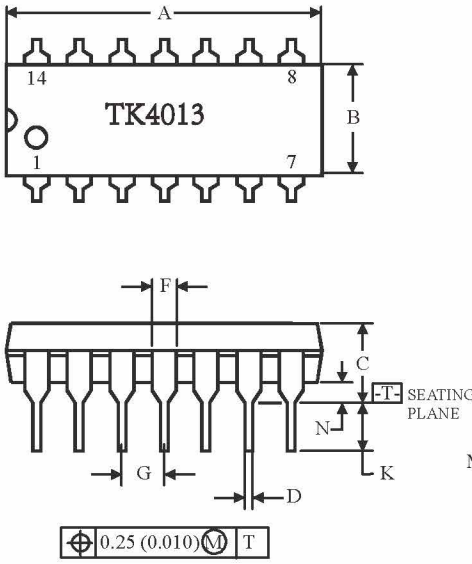
Figure 3. Switching Waveforms

■ EXPANDED LOGIC DIAGRAM
(1/2 of the Device)



N SUFFIX PLASTIC DIP
(MS - 001AA)



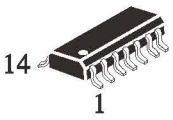


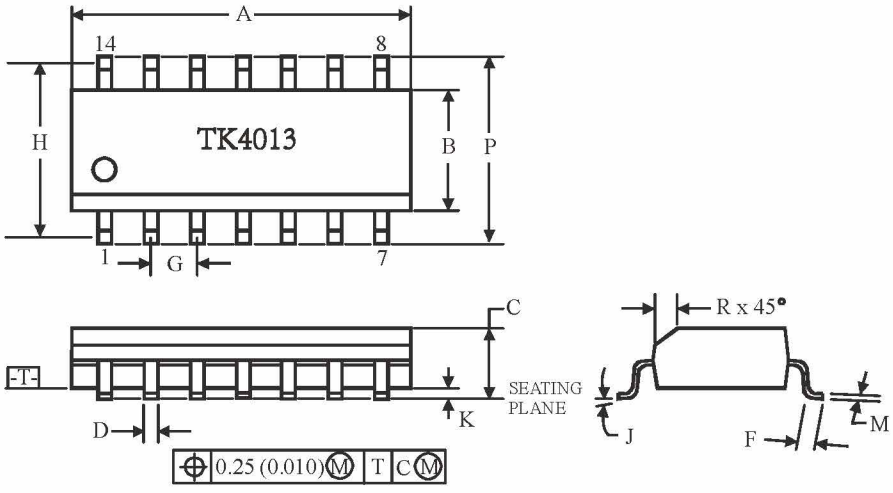
Symbol	Dimensions, mm	
	MIN	MAX
A	18.67	19.69
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions. Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AB)





Symbol	Dimensions, mm	
	MIN	MAX
A	8.55	8.75
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

1.Dimensions A and B do not include mold flash or protrusion.
2.Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.