I²C-Compatible (Two-Wire) Serial EEPROM 8Kbit (1,024 x 8)

Description

The TK24C08C provides 8,192 of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 1,024 words of 8 bits each. The device's cascading feature allows up to TK24C08C to share a common two-wire bus. These devices are optimized for use in many industrial and commercial applications where low power and low voltage operations are essential. The devices are available in space-saving SOIC-8, TSSOP-8, PDIP-8 packages. All packages operate from 1.7V to 5.5V.

Features

- Internally Organized as 1,024 x 8 (8K)
- Industrial Temperature Range: -40°C to +85°C
- I²C-Compatible (Two-Wire) Serial Interface:100 kHz Standard mode, 400 kHz Fast mode, 1 MHz (FM+)
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Write-Protect Pin for Full Array Hardware Data Protection
- Ultra Low Active Current (3 mA maximum) and Standby Current (6 µA maximum)
- 16-byte Page Write Mode: Partial page writes allowed
- High Reliability: Endurance: 1,000,000 write cycles Data retention: 100 years
- ESD Protection > 4,000V
- Random and Sequential Read Modes
- Self-Timed Write Cycle within 5 ms Maximum

Ordering Information

Part Number	Package	Packing	Temperature(TA)	Package Qty	Note
TK24C08C-G	TSSOP-8	Reel	-40°C ~ 85°C	5000	
TK24C08C-A	SOIC-8	Reel	-40°C ~ 85°C	2500	
TK24C08C-D	DIP-8	Tube	-40°C ~ 85°C	1000	

Electrical Characteristics

Absolute Maximum Ratings

Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

V_{CC}.....6.25V

Voltage on any pin with respect to ground.....-1.0V to +7.0V

ESD protection.....>4 kV

DC output current.....5.0 mA

Temperature under bias.....-55°C to +125°C

Storage temperature.....-65°C to +150°C

DC and AC Operating Range

Table1. DC and AC Operating Range

Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low Voltage Grade	1.7V to 5.5V

DC Characteristics

Table2. DC Characteristics

Parameter	Symbol	Minimum	Typical(1)	Maximum	Units	Test Conditions
Supply Voltage	V_{CC}	1.7	—	5.5	V	
Supply Current	I_{CC1}	—	0.4	1.0	mA	V_{CC} = 5.0V, Read at 100 kHz
Supply Current	I_{CC2}	—	2.0	3.0	mA	V_{CC} = 5.0V, Write at 100 kHz
Standby Current	I_{SB}	—	—	1.0	µA	V_{CC} = 1.7V, V_{IN} = V_{CC} or GND
		—	—	6.0	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND
Input Leakage	I_{LI}	—	0.10	3.0	µA	V_{IN} = V_{CC} or GND
Output Leakage	I_{LO}	—	0.05	3.0	µA	V_{OUT} = V_{CC} or GND
Input Low Level	V_{IL}	-0.6	—	V_{CC} x 0.3	V	
Input High Level	V_{IH}	V_{CC} x 0.7	—	V_{CC} + 0.5	V	
Output Low Level	V_{OL1}	—	—	0.2	V	V_{CC} = 1.7V, I_{OL} = 0.15 mA
Output Low Level	V_{OL2}	—	—	0.4	V	V_{CC} = 3.0V, I_{OL} = 2.1 mA

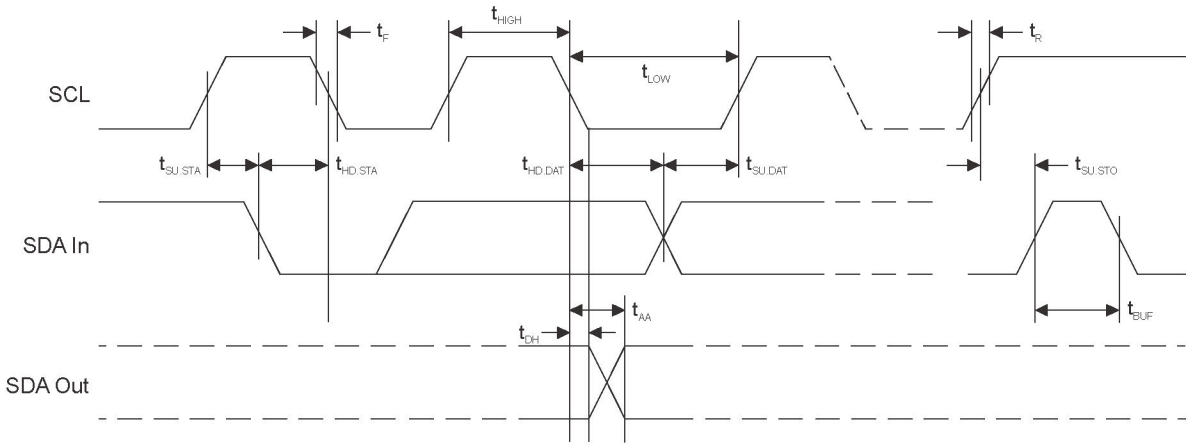
AC Characteristics

measurement conditions:CL: 100 pF,RPUP (SDA bus line pull-up resistor to VCC): 1.3 kΩ (1000 kHz), 4 kΩ (400 kHz),10 kΩ (100 kHz)
Input and output timing reference voltages: 0.5 x V_{CC},Input rise and fall times: ≤50 ns

Table3. AC Characteristics

Parameter	Symbol	Fast Mode		Fast Mode Plus		Units
		V_{CC} = 1.7V to 2.5V		V_{CC} = 2.5V to 5.5V		
		Min.	Max.	Min.	Max.	
Clock Frequency, SCL	f_{SCL}	—	400	—	1000	kHz
Clock Pulse Width Low	t_{LOW}	1,200	—	500	—	ns
Clock Pulse Width High	t_{HIGH}	600	—	400	—	ns
Input Filter Spike Suppression	t_I	—	100	—	50	ns
Clock Low to Data Out Valid	t_{AA}	100	900	50	450	ns
Bus Free Time between Stop and Start	t_{BUF}	1,200	—	500	—	ns
Start Hold Time	$t_{HD.STA}$	600	—	250	—	ns
Start Set-up Time	$t_{SU.STA}$	600	—	250	—	ns
Data In Hold Time	$t_{HD.DAT}$	0	—	0	—	ns
Data In Set-up Time	$t_{SU.DAT}$	100	—	100	—	ns
Inputs Rise Time	t_R	—	300	—	300	ns
Inputs Fall Time	t_F	—	300	—	100	ns
Stop Set-up Time	$t_{SU.STO}$	600	—	250	—	ns
Data Out Hold Time	t_{DH}	50	—	50	—	ns
Write Cycle Time	t_{WR}	—	5	—	5	ms

Figure1. Bus Timing



Electrical Specifications

Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the TK24C08C should monotonically rise from GND to the minimum V_{CC} level, as specified in Table1, with a slew rate no faster than 0.1 V/ µs.

Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the TK24C08C includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus master must wait at least t_{PUP} before sending the first command to the device. See Table4 for the values associated with these power-up parameters.

Table4. Power-up Conditions

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands	100	—	µs
V_{POR}	Power-on Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	500	—	ms

Pin Capacitance

Table5. Pin Capacitance

Symbol	Test Condition	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A1, A2 and SCL)	6	pF	V_{IN} = 0V

EEPROM Cell Performance Characteristics

Table6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance	T_A = 25°C, V_{CC} = 3.3V, Page Write mode	1,000,000	—	Write Cycles
Data Retention	T_A = 55°C	100	—	Years

Device Operation and Communication

The TK24C08C operates as a slave device and utilizes a simple I^2C-compatible two-wire digital serial interface to communicate with a host controller, commonly referred to as the bus master. The master initiates and controls all read and write operations to the slave devices on the serial bus, and both the master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the master, while the bidirectional SDA pin is used to receive command and data information from the master as well as to send data back to the master. Data is always latched into the TK24C08C on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant bit (MSb) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an Acknowledge (ACK) or a No-Acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the master and the slave devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the master. In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic-high state at the same time.

Clock and Data Transition Requirements

The SDA pin is an open-drain terminal and therefore must be pulled high with an external pull-up resistor. SCL is an input pin that can either be driven high or pulled high using an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below. The relationship of the AC timing parameters with respect to SCL and SDA for the TK24C08C are shown in the timing waveform in Figure1. The AC timing characteristics and specifications are outlined in AC Characteristics.

Start and Stop Conditions

Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable logic '1' state and will bring the device out of Standby mode. The master uses a Start condition to initiate any data transfer sequence; therefore, every command must begin with a Start condition.
The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Refer to Figure 2 for more details.

Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic '1' state.
The master can use the Stop condition to end a data transfer sequence with the TK24C08C which will subsequently return to Standby mode. The master can also utilize a repeated Start condition instead of a

Stop condition to end the current data transfer if the master will perform another operation. Refer to Figure 2 for more details.

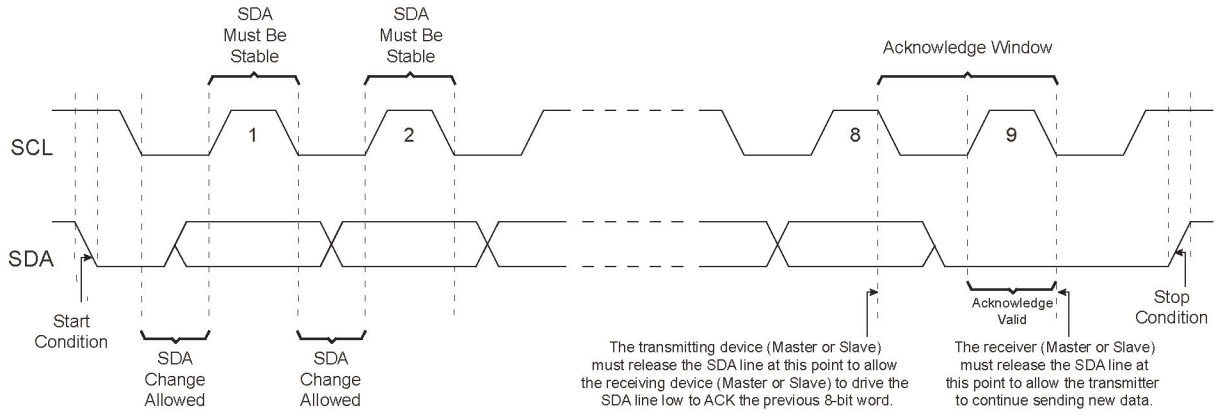
Acknowledge and No-Acknowledge

After every byte of data is received, the receiving device must confirm to the transmitting device that it has successfully received the data byte by responding with what is known as an Acknowledge (ACK). An ACK is accomplished by the transmitting device first releasing the SDA line at the falling edge of the eighth clock cycle followed by the receiving device responding with a logic '0' during the entire high period of the ninth clock cycle.

When the TK24C08C is transmitting data to the master, the master can indicate that it is done receiving data and wants to end the operation by sending a logic '1' response to the TK24C08C instead of an ACK response during the ninth clock cycle. This is known as a No-Acknowledge (NACK) and is accomplished by the master sending a logic '1' during the ninth clock cycle, at which point the TK24C08C will release the SDA line so the master can then generate a Stop condition.

The transmitting device, which can be the bus master or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a logic '0' to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram has been provided in Figure 2 to better illustrate these requirements.

Figure 2. Start Condition, Data Transitions, Stop Condition and Acknowledge



Standby Mode

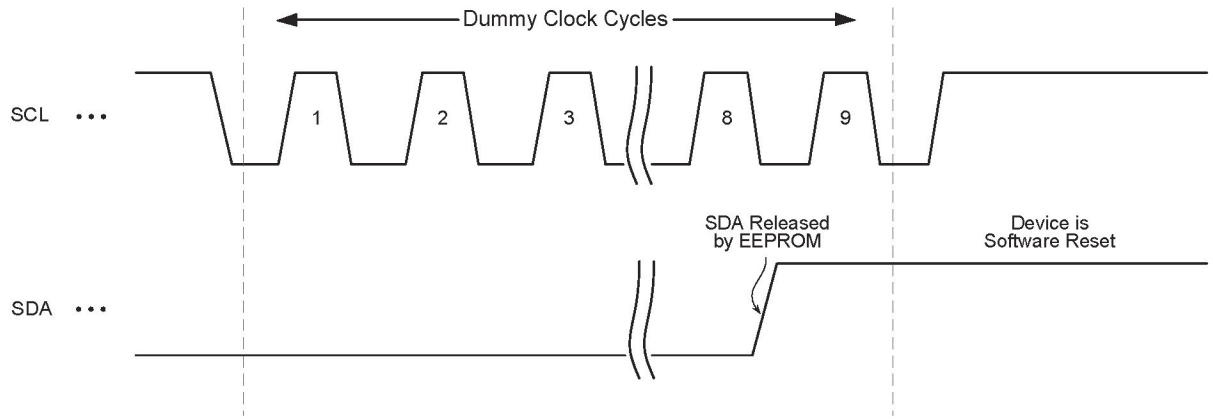
The TK24C08C features a low-power Standby mode that is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see Power-Up Requirements and Reset Behavior).
- A Stop condition is received by the device unless it initiates an internal write cycle (see Write Operations).
- At the completion of an internal write cycle (see Write Operations).

Software Reset

After an interruption in protocol, power loss or system Reset, any two-wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The software Reset sequence should not take more than nine dummy clock cycles. Once the software Reset sequence is complete, new protocol can be sent to the device by sending a Start condition followed by the protocol. Refer to Figure 3 for an illustration.

Figure 3. Software Reset



In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see Power-Up Requirements and Reset Behavior).

Memory Organization

The TK24C08C is internally organized as 64 pages of 16 bytes each.

Device Addressing

TK24C08C Device Addressing

Accessing the device requires an 8-bit device address byte following a Start condition to enable the device for a read or write operation. Since multiple slave devices can reside on the serial bus, each slave device must have its own unique address so the master can access each device independently.

The Most Significant four bits of the device address byte is referred to as the device type identifier. The device type identifier '1010' (Ah) is required in bits 7 through 4 of the device address byte (see Table 7).

Following the 4-bit device type identifier is the hardware slave address bit, A2. This bit can be used to expand the address space by allowing up to two Serial EEPROM devices on the same bus. The A2 value must correlate with the voltage level on the corresponding hardwired device address input pin A2. The A2 pin uses an internal proprietary circuit that automatically biases it to a logic '0' state if the pin is allowed to float. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once the pin is biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. TTESEMI recommends connecting the A2 pin to a known state whenever possible.

Following the A2 hardware slave address bit are bits A9 and A8 (bit 2 and bit 1 of the device address byte), which are the two Most Significant bits of the memory array word address. Refer to Table 7 to review these bit positions.

The eighth bit (bit 0) of the device address byte is the Read/Write Select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon the successful comparison of the device address byte, the TK24C08C will return an ACK. If a valid comparison is not made, the device will NACK.

Table 7. TK24C08C Device Address Byte

Package	Device Type Identifier				Hardware Slave Address Bit	Most Significant Bits of the Word Address		R/W Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOIC, TSSOP, PDIP,	1	0	1	0	A2	A9	A8	R/$\overline{W}$

For all operations except the current address read, a word address byte must be transmitted to the device immediately following the device address byte. The word address byte consists of the remaining eight bits of the 10-bit memory array word address, and is used to specify which byte location in the EEPROM to start reading or writing. Refer to Table 8 to review these bit positions.

Table8. TK24C08C Word Address Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A7	A6	A5	A4	A3	A2	A1	A0

Device Default Condition

The TK24C08C is delivered with the EEPROM array set to logic '1', resulting in FFh data in all locations.

Write Operations

All write operations for the TK24C08C begin with the master sending a Start condition,followed by a device address byte with the R/W bit set to logic '0', and then by the word address byte. The data value(s) to be written to the device immediately follow the word address byte.

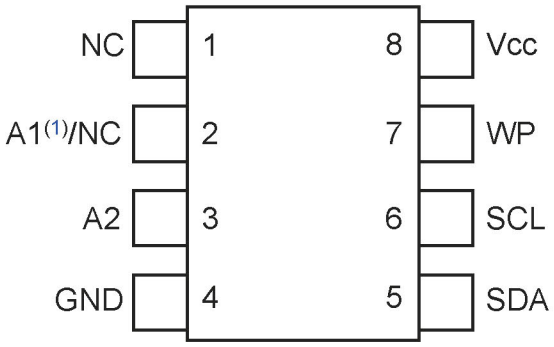
Read Operations

Read operations are initiated the same way as write operations with the exception that the Read/Write Select bit in the device address byte must be a logic '1'. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Pin Functions

PDIP/SOIC/TSSOP
(Top View)



1. This pin is device address input (A1) pin on the TK24C08C and is a NC or no connect on the TK24C08C.

Pin Description

Name	8-Lead PDIP	8-Lead SOIC	8-Lead TSSOP	Function
NC	1	1	1	No Connect
A1/NC	2	2	2	Device Address Input/ No Connect
A2	3	3	3	Device Address Input
GND	4	4	4	Ground
SDA	5	5	5	Serial Data
SCL	6	6	6	Serial Clock
WP	7	7	7	Write-Protect
V_{CC}	8	8	8	Device Power Supply

Note:

If the A1, A2 or WP pins are not driven, they are internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. TTESEMI recommends connecting these pins to a known state whenever possible.

Device Address Inputs (A1, A2)

The A1 and A2 pins are device address inputs that are hard-wired (directly to GND or to V_{CC}) for compatibility with other two-wire Serial EEPROM devices. When the pins are hard-wired on the TK24C08C, as many as four devices may be addressed on a single bus system. A device is selected when a corresponding hardware and software match is true. If the pins are left floating, the A1 and A2 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, TTESEMI recommends always connecting the address pins to a known state. When using a pull-up resistor, TTESEMI recommends using 10 kΩ or less.

Ground

The ground reference for the power supply. GND should be connected to the system ground.

Serial Data (SDA)

The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled high using an external pull-up resistor (not to exceed 10 kΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

Serial Clock (SCL)

The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled high using an external pull-up resistor.

Write-Protect (WP)

The write-protect input, when connected to GND, allows normal write operations. When the WP pin is connected directly to V_{CC}, all write operations to the protected memory are inhibited.

If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, TTESEMI recommends always connecting the WP pin to a known state. When using a pull-up resistor, TTESEMI recommends using 10 kΩ or less.

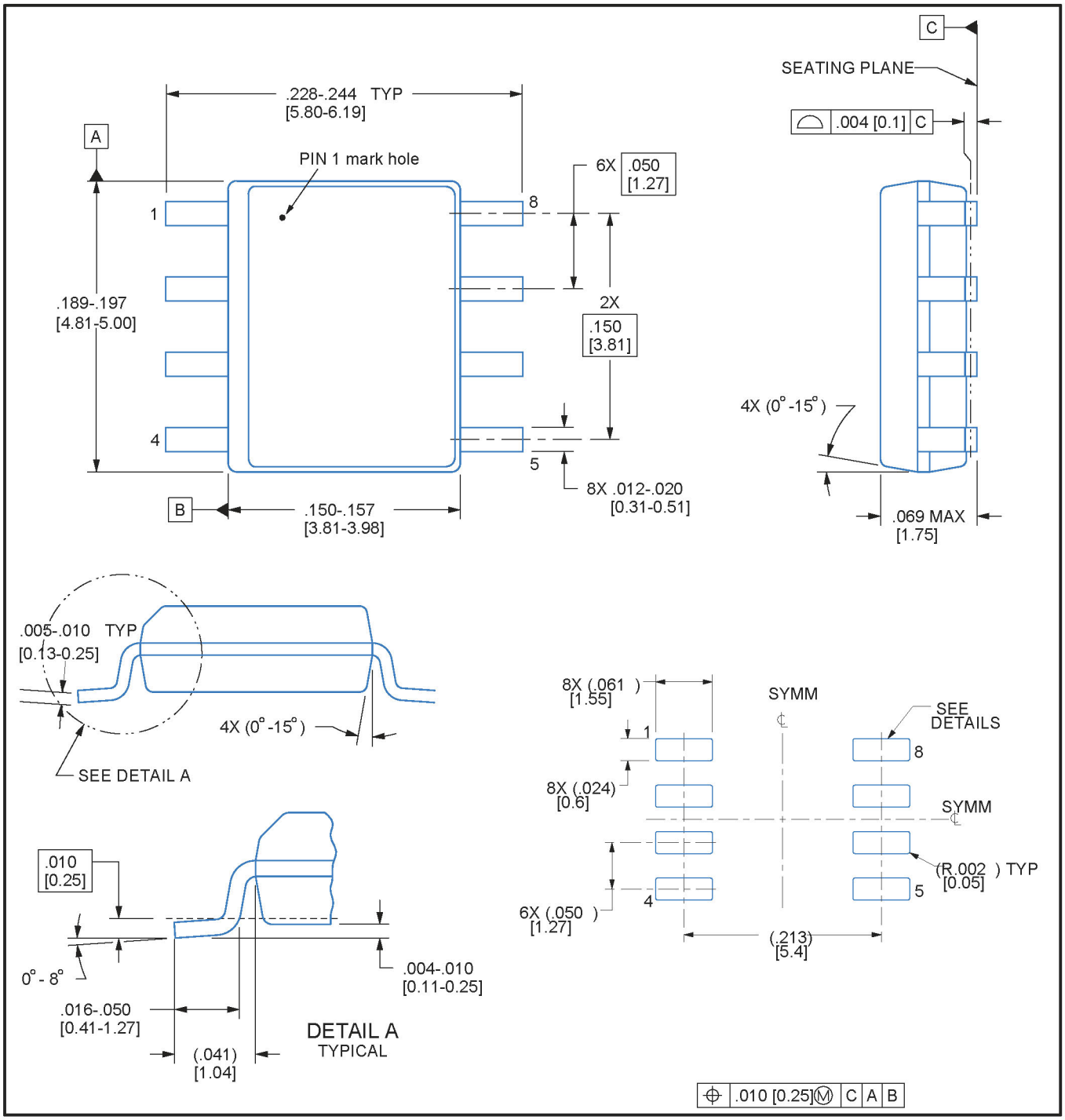
Table 8. Write-Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Full Array
At GND	Normal Write Operations

Device Power Supply

The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

PACKAGE OUTLINE SOIC - 8,1.75 mm max height



NOTES: Linear dimensions are in inches [millimeters]. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.