High speed Low-Power CAN transceiver

■ Description

The TK1050 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus.
The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.
As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (M/bps).
The TK1050 is designed for operation in especially harsh environments. As a result, the device features cross-wire, overvoltage and loss of ground protection from –27V to 40V, overtemperature shutdown, a –12V to 12V common-mode range, and will withstand voltage transients from –200V to 200V according to ISO7637.

■ Features

- Fully compatible with the ISO 11898 standard
- At least 110 nodes can be connected
- Improved Replacement for the TJA1050
- ±12 kV ESD Protection
- Bus-Fault Protection of -50V to 50V
- Thermally protected
- Transmit Data (TXD) dominant time-out function
- High speed (up to 1 MBaud)
- Silent mode in which the transmitter is disabled

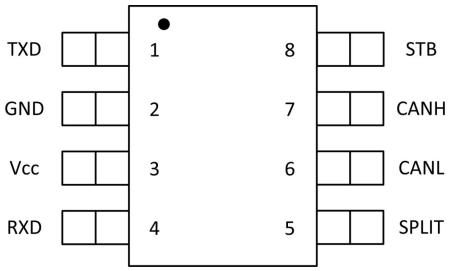
■ Applications

- Industrial Automation
- High-Speed CAN Bus for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface

■ Ordering Information

Ordering Number	Package	Packing
TK1050TR	SOP8	Reel

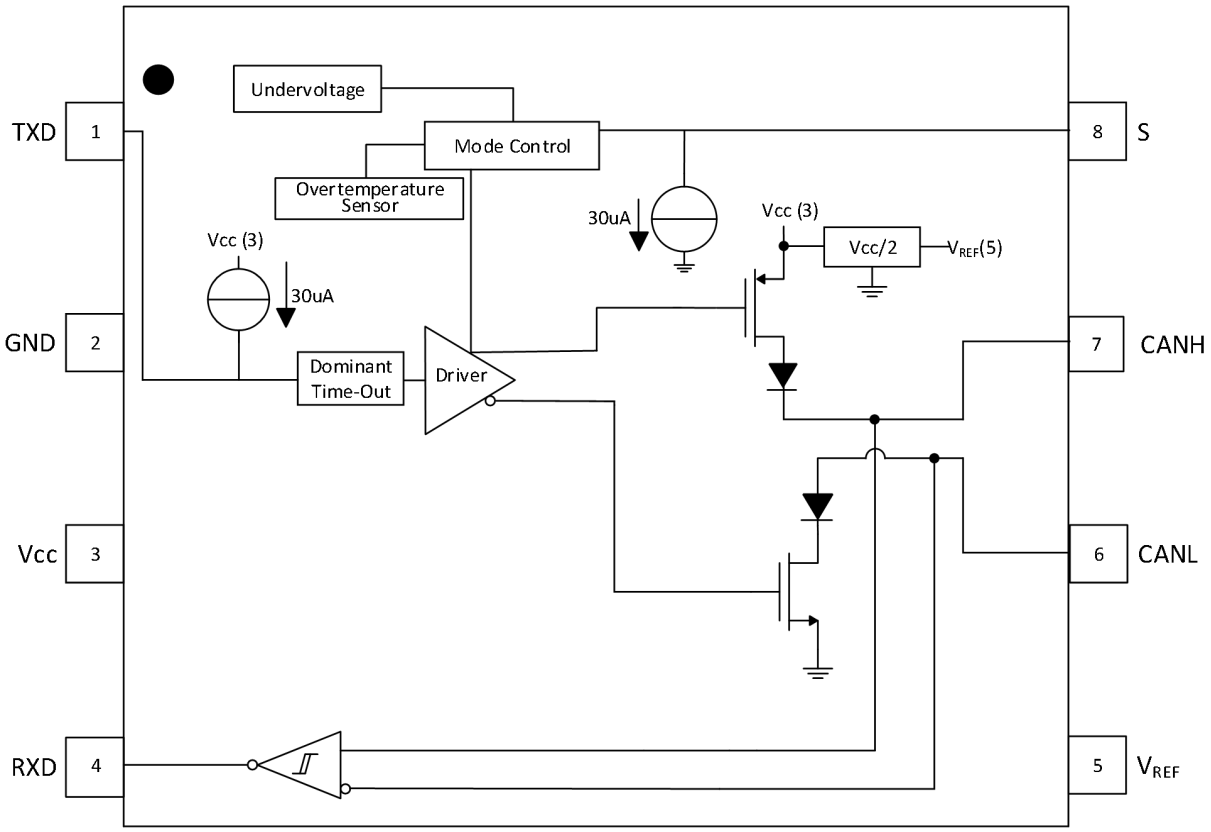
■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin		I/O	Description
No.	Name		
1	TXD	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	GND	Device ground
3	V_{CC}	Supply	Transceiver 5-V supply
4	RXD	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	SPLIT	O	Reference output voltage
6	CANL	I/O	Low level CAN bus line
7	CANH	I/O	High level CAN bus line
8	STB	I	Mode select: Strong pull down to GND for high speed mode, strong pull up to VCC for low power mode

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25ºC, unless otherwise specified)

Parameter	Description	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	7	V
	Voltage at any bus terminal (CANH, CANL, V_{ref})	-50	50	V
V_I	Voltage input, transient pulse(2)(CANH, CANL)	-200	200	V
V_I	Voltage input range (TXD, S)	-0.5	6	V
T_J	Junction temperature	-55	170	℃
T_{stg}	Storage temperature	-40	125	℃

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5V, T_A=-25℃ ~ 125℃, unless otherwise specified)

Recommended Operating Condition

Parameter	Description		Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		-24	24	V
V_{IH}	High-level input voltage	TXD, S	2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{ID}	Differential input voltage		-7	7	V
I_{OH}	High-level output current	Driver	-70		mA
		Receiver	-6		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver		6	
T_J	Junction temperature	See Absolute Maximum Ratings(1), 1-Mbps minimum signaling rate with RL = 54Ω	-40	150	℃
	Signaling Rate		20		kbps

Driver Electronical Characteristics

Parameter	Description		Test Conditions		Min	TYP(1)	Max	Unit
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	V_I = 0V, S at 0V, R_L = 60 Ω, See Figure 1 and Figure 2	4.75V < V_{CC} < 5.25V	3.0	3.6	4.5	V
				4.5V < V_{CC} < 5.5V	2.75		5.2	
		CANL		4.75V < V_{CC} < 5.25V	0.8	1.4	1.6	
				4.5V < V_{CC} < 5.5V			1.6	
$V_{O(R)}$	Bus output voltage (Recessive)		V_I = 3V, S at 0V, R_L = 60 Ω,See Figure 1 and Figure 2	4.75V < V_{CC} < 5.25V	2	2.5	3	V
				4.5V < V_{CC} < 5.5V	1.8	2.4	3	V
$V_{OD(D)}$	Differential output voltage (Dominant)		V_I = 0V, R_L = 60 Ω, S at 0V,See Figure 1 and Figure 2,and Figure 3	4.75V < V_{CC} < 5.25V	1.5	2.2	3	V
				4.5V < V_{CC} < 5.5V	1.4		3	
			V_I = 0V, R_L = 45 Ω, S at 0V,See Figure 1 and Figure 2,and Figure 3	4.75V < V_{CC} < 5.25V	1.4		3	
				4.5V < V_{CC} < 5.5V	1.3		3	
$V_{OD(R)}$	Differential output voltage (Recessive)		V_I = 3V, S at 0V,See Figure 1 and Figure 2		-0.012		0.012	V
			V_I = 3V, S at 0V, No Load		-0.5		0.05	
$V_{OC(SS)}$	Steady state common-mode output voltage		S at 0V	4.75V < V_{CC} < 5.25V	2	2.5	3	V
				4.5V < V_{CC} < 5.5V	1.9		3	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage					30		mV

■ ELECTRICAL CHARACTERISTICS (Cont.)

I_{IH}	High-level input current, TXD input	V_I at V_{CC}	-2	0	2	μA
I_{IL}	Low-level input current, TXD input	V_I at 0V	-50	-30	-10	
$I_{O(off)}$	Power-off TXD output current	V_{CC} at 0V, TXD at 5V			1	
$I_{OS(SS)}$	Short-circuit steady-state output current	V_{CANH} = - 12V, CANL Open	-130	-100		mA
		V_{CANH} = 12V, CANL Open			1	
		V_{CANL} = - 12V, CANH Open	-1			
		V_{CANL} = 12V, CANH Open		77	105	
C_O	Output capacitance	See receiver input capacitance				

Receiver Electronical Characteristics

Parameter	Description	Test Conditions		Min	TYP(1)	Max	Unit
V_{IT+}	Positive-going input threshold voltage	S at 0V			800	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})			100	125		
V_{OH}	High-level output voltage	I_O = -2mA See Figure 6	4.75V < V_{CC} < 5.25V	4	4.6		V
			4.5V < V_{CC} < 5.5V	3.8			
V_{OL}	Low-level output voltage	I_O = 2mA,See Figure 6			0.3	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH or CANL = 5V, Other pin at 0V, V_{CC} at 0V, TXD at 0V			165	250	μA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0V, RXD at 5V				20	μA
C_I	Input capacitance to ground, (CANH or CANL)	TXD at 3 V, V_I = 0.4sin (4E6πt) + 2.5 V			13		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4sin (4E6πt)			5		
R_{ID}	Differential input resistance	TXD at 3V, S at 0V		30	50	80	kΩ
R_{IN}	Input resistance, (CANH or CANL)			15	25	40	
$R_{I(m)}$	Input resistance matching [1 - $R_{IN\ (CANH)}$ / $R_{IN\ (CANL))}$] x 100%	$V_{(CANH)}$ = $V_{(CANL)}$		-3%	0	3%	

Device Switching Characteristics

Parameter	Description	Test Conditions		Min	TYP	Max	Unit
$T_{d(LOOP1)}$	Total loop delay, driver input to receiver output, Recessive to Dominant	S at 0V	4.75V < VCC < 5.25V	70	100	190	ns
			4.5V < VCC < 5.5V	75		115	
$T_{d(LOOP2)}$	Total loop delay, driver input to receiver output, Dominant to Recessive		4.75V < VCC < 5.25V	70	110	190	
			4.5V < VCC < 5.5V	75		155	

Driver Switching Characteristics

Parameter	Description	Test Conditions		Min	TYP	Max	Unit
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0V, See Figure 4		25	55	110	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	50	90	
t_r	Differential output signal rise time			25			
t_f	Differential output signal fall time			50			
t_{en}	Enable time from silent mode to dominant					10	μs
$T_{(dom)}$	Dominant time-out	↓V_I	4.75V < V_{CC} < 5.25V	300	550	700	μs
			4.5V < V_{CC} < 5.5V	280		700	

■ ELECTRICAL CHARACTERISTICS (Cont.)

Receiver Switching Characteristics

Parameter	Description	Test Conditions		Min	TYP	Max	Unit
T_{PLH}	Propagation delay time, low-to-high-level output	S at 0V or V_{CC} See Figure 6	4.75V < V_{CC} < 5.25V	50	75	130	ns
			4.5V < V_{CC} < 5.5V	55		135	
T_{PHL}	Propagation delay time, high-to-low-level output		4.75V < V_{CC} < 5.25V	25	50	90	
			4.5V < V_{CC} < 5.5V	30		95	
t_r	Output signal rise time			8			
t_f	Output signal fall time			8			

Dissipation Ratings

Parameter	Description	Min	Typ	Max	Unit
T_{JS}	Junction Temperature, Thermal Shutdown		190		℃

Supply Current

Parameter	Description		Test Conditions		Min	TYP	Max	Unit
I_{CC}	5-V Supply current	Silent mode	S at V_{CC}, V_I = V_{CC}			2.5	5	mA
		Dominant	V_I = 0V, 60 Ω Load, S at 0V	4.75V < V_{CC} < 5.25V		50	70	
				4.5V < V_{CC} < 5.5V			75	
		Recessive	V_I = V_{CC}, No Load, S at 0V			2.5	5	

Split-Pin Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{IH}	High level input current	S at 2V	20	35	50	μA
I_{IL}	Low level input current	S at 0.8V	15	30	45	

VREF-Pin Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{REF}	Reference output voltage	–50 μA < I_O < 50 μA	0.4V_{CC}	0.5V_{CC}	0.6V_{CC}	V

ESD Ratings

			Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±8000	V
		Bus terminals vs GND	±12000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±2000	
	Machine model (MM) ANSI/ESDS5.2-1996		±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

■ PARAMETER MEASUREMENT INFORMATION

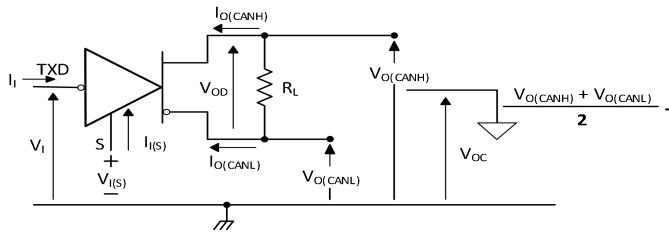


Figure 1. Driver Voltage, Current, and Test Definition

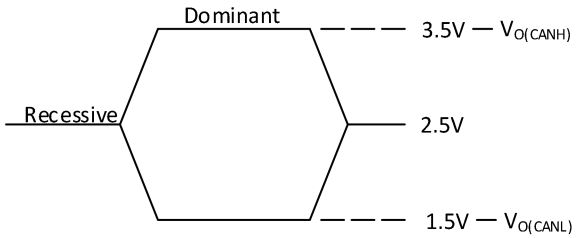


Figure 2. Bus Logic State Voltage Definitions

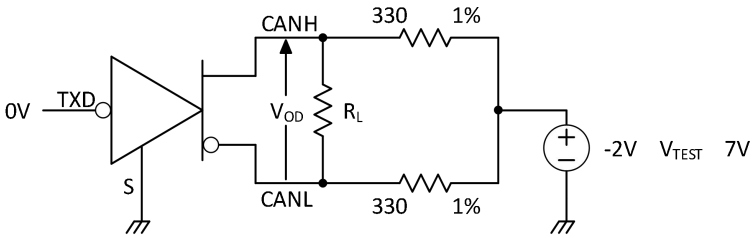


Figure 3. Driver VOD Test Circuit

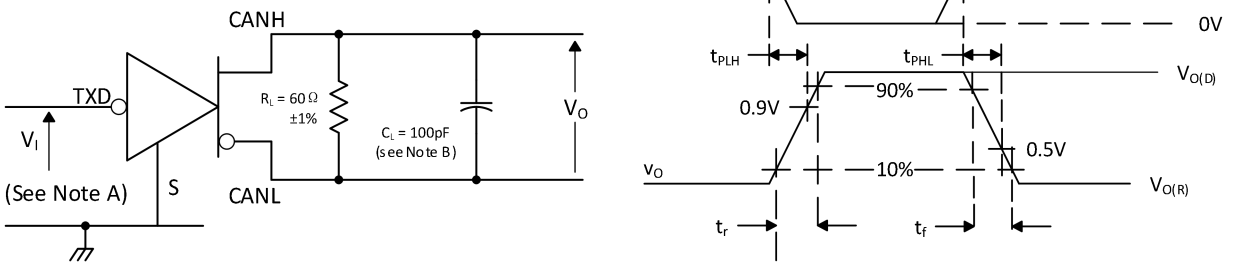


Figure 4. Driver Test Circuit and Voltage Waveforms

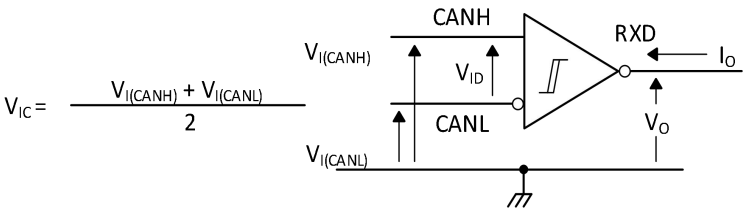
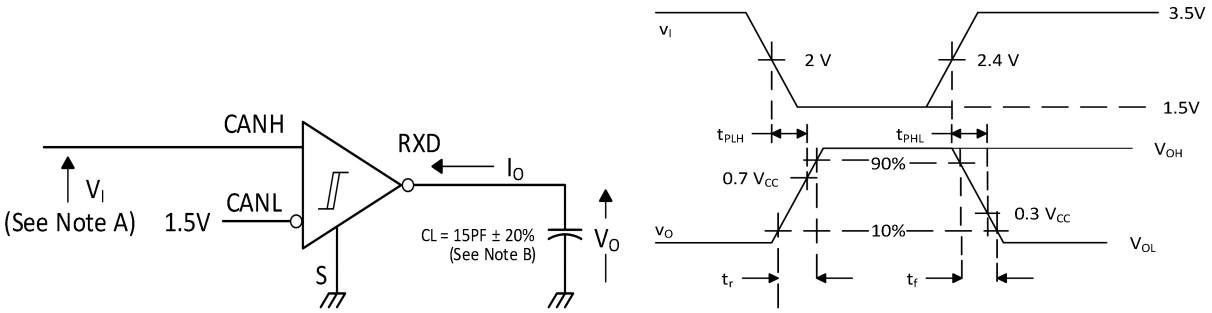


Figure 5. Receiver Voltage and Current Definitions

■ PARAMETER MEASUREMENT INFORMATION (CONTINUED)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns,t_f ≤ 6ns, Z_O = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 2. **Driver Truth Table**

INPUTS		OUTPUTS		BUS STATE
TXD(1)	S(1)	CANH(1)	CANL(1)	
L	L or Open	H	L	DOMINANT
H	X	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; Z = high impedance

Table 3. **Receiver Truth Table**

DIFFERENTIAL INPUTS V_{ID} = V(CANH) - V(CANL)	OUTPUT RXD(1)	BUS STATE
V_{ID} ≥ 0.9 V	L	DOMINANT
0.5V < V_{ID} < 0.9V	?	?
V_{ID} ≤ 0.5V	H	RECESSIVE
Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

■ APPLICATION AND IMPLEMENTATION

Application Information

The CAN bus has two states during powered operation of the device; dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD pin. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal resistors R_{IN} and R_{ID} of the receiver, corresponding to a logic high on the TXD and RXD pins. See Figure 7 and Figure 8.

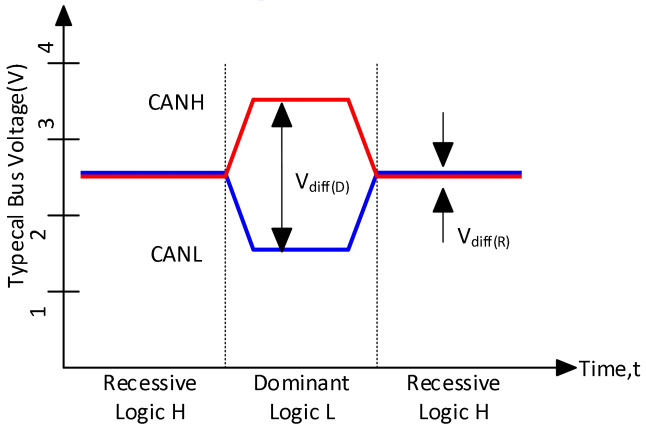


Figure 7. Bus States

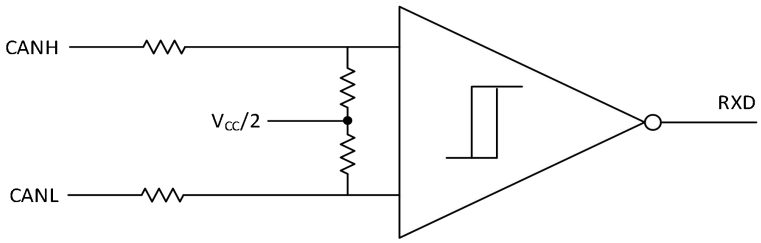


Figure 8. Simplified Recessive Common Mode Bias and Receiver

CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120Ω characteristic impedance twisted-pair cable with termination on both ends of the bus.

■ TYPICAL APPLICATION

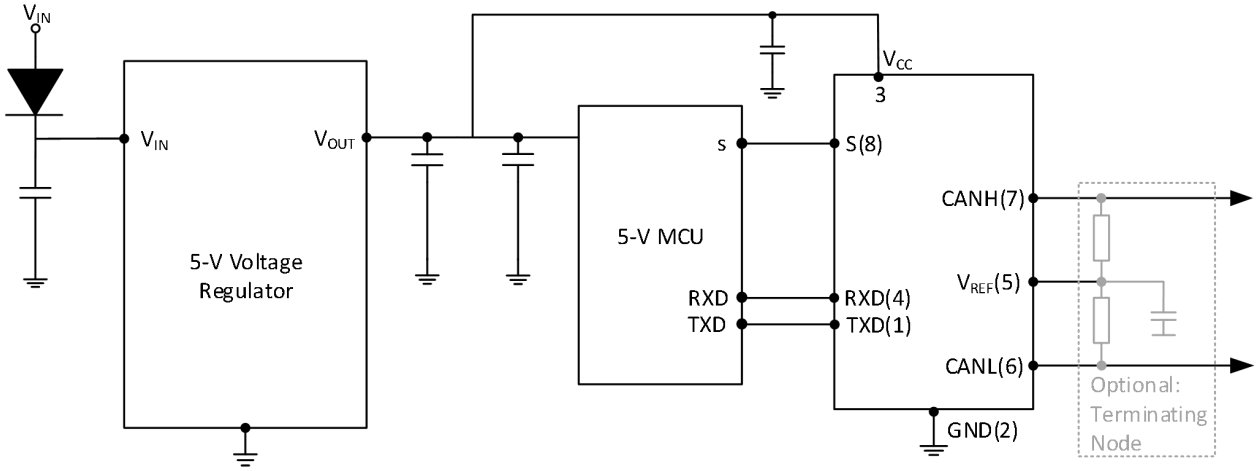


Figure 9. Typical Application Schematic

Design Requirements

Bus Loading, Length, and Number of Nodes

The ISO11898 Standard specifies up to 1Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are SAE J1939, CAN open, Device Net and NMEA2000.

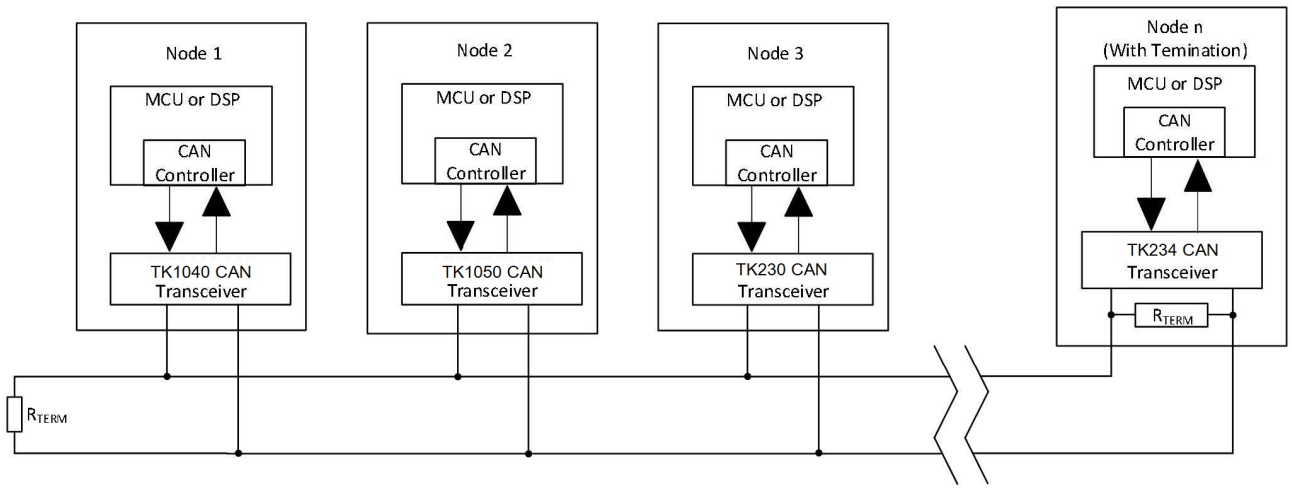


Figure 10. Typical CAN Bus

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the TK1050 CAN transceiver. ISO11898-2 specifies the driver differential output with a 60-Ω load (two 120Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The TK1050 device is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common mode range of –2 V to 7 V via a 330-Ω coupling network. This network represents the bus loading of 90 TK1050 transceivers based on their minimum differential input resistance of 30kΩ. Therefore, the TK1050 supports up to 90 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1-km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard.

CAN Termination

The ISO11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Termination is typically a 120Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 11). Split termination uses two 60Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Care should be taken when determining the power ratings of the termination resistors. A typical worst case fault condition is if the system power supply and ground were shorted across the termination resistance which would result in much higher current through the termination resistance than the current limit of the CAN transceiver.

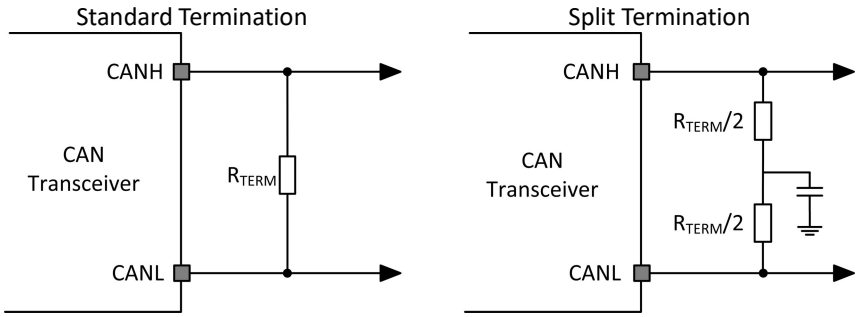
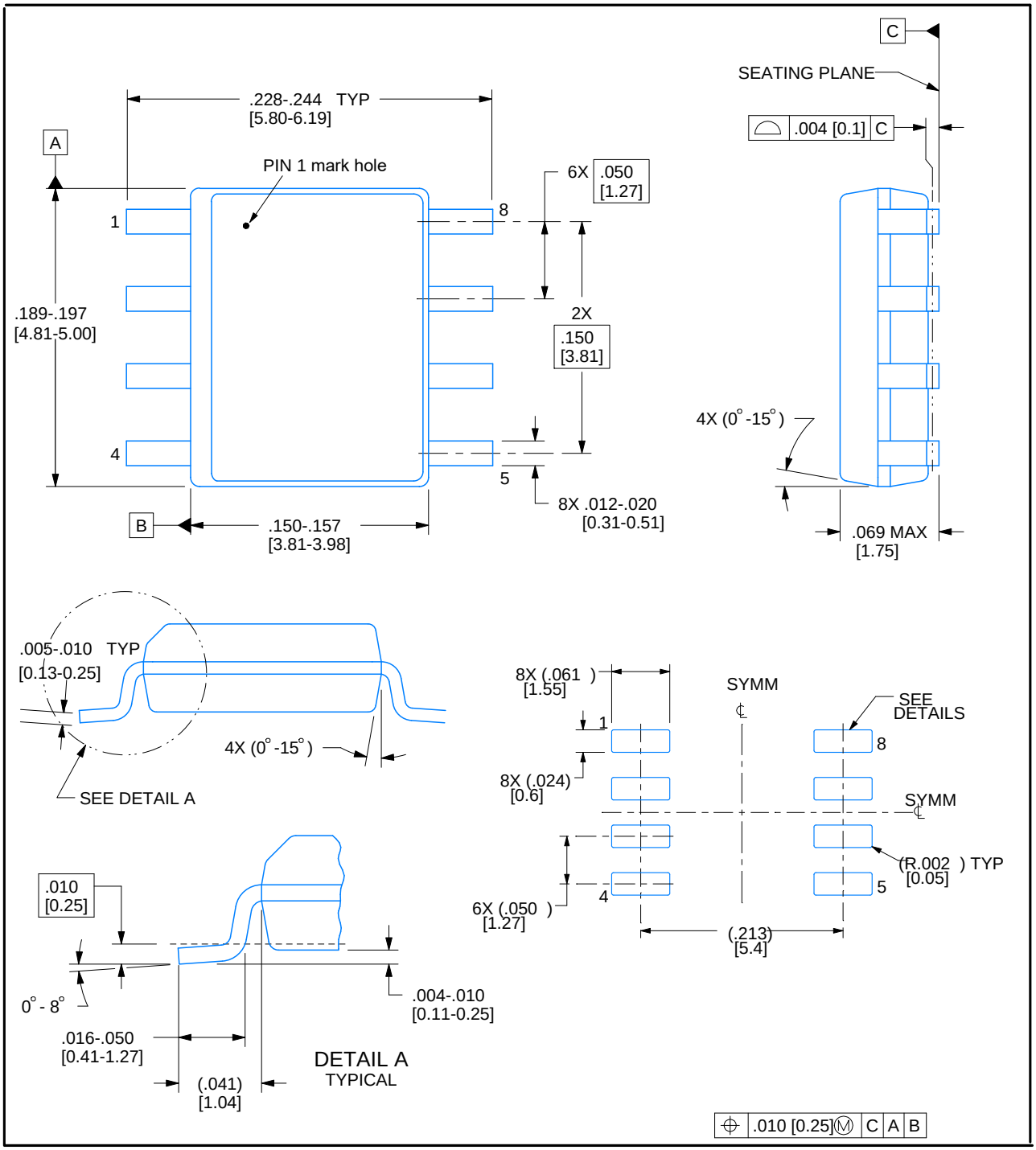


Figure 11. CAN Termination

Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (TXD pin) to the differential outputs (CANH and CANL pins), plus the delay from the receiver inputs (CANH and CANL) to its output (RXD pin).

PACKAGE OUTLINE SOIC - 8,1.75 mm max height



NOTES: Linear dimensions are in inches [millimeters]. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.