

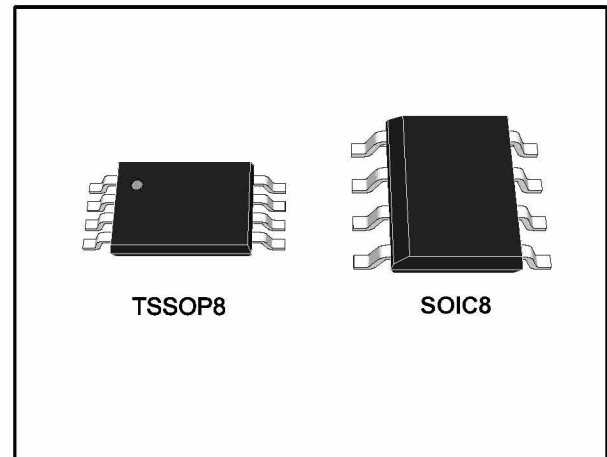
## Low-power dual operational amplifiers

### Description

These circuits consist of two independent, high-gain, internally frequency-compensated op amps, specifically designed to operate from a single power supply over a wide range of voltages. The low-power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard 5 V, which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.



### Features

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 0.7 MHz (temperature compensated)
- Very low supply current per channel essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 3 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing  
0 V to ( $V_{CC^+} - 1.5$  V)

### Applications

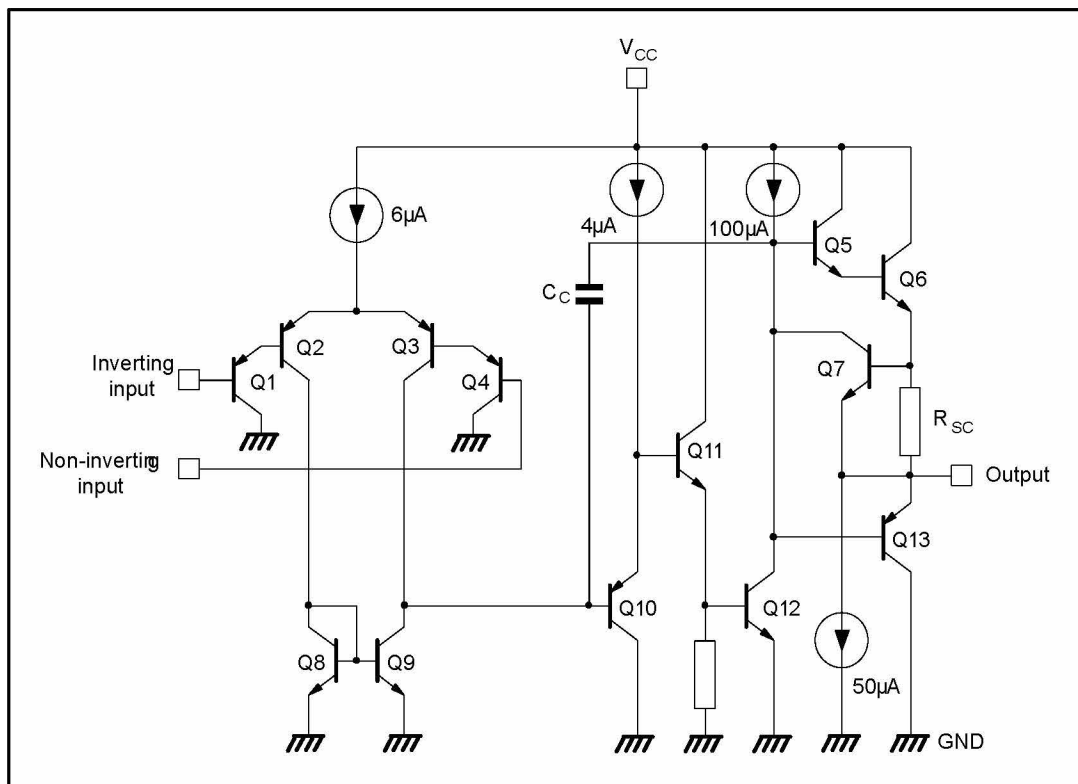
- Merchant network and server power supply units
- Multi-function printers
- Power supplies and mobile chargers
- Motor control: AC induction, brushed DC
- Desktop PC and motherboard
- Indoor and outdoor air conditioners
- Washers, dryers, and refrigerators
- AC inverters, string inverters, central inverters, and voltage frequency drives
- Uninterruptible power supplies
- Electronic point-of-sale systems

## 1 Ordering information Table 1.

Part Number	Package	Packing	Temperature (TA)	Package Qty	Note
LM158DT	SOIC-8	Reel	-55°C ~ 125°C	2500	
LM258DR	SOIC-8	Reel	-25°C~85°C	2500	
LM258ADR	SOIC-8	Reel	-25°C~85°C	2500	
LM358DR	SOIC-8	Reel	0°C~70°C	2500	
LM358ADR	SOIC-8	Reel	0°C~70°C	2500	
LM358PWR	TSSOP-8	Reel	0°C~70°C	2500	

## 2 Schematic diagram

Figure 1: Schematic diagram (1/2 LM158)



### 3 Package pin connections

Figure 2: Pin connections (top view)

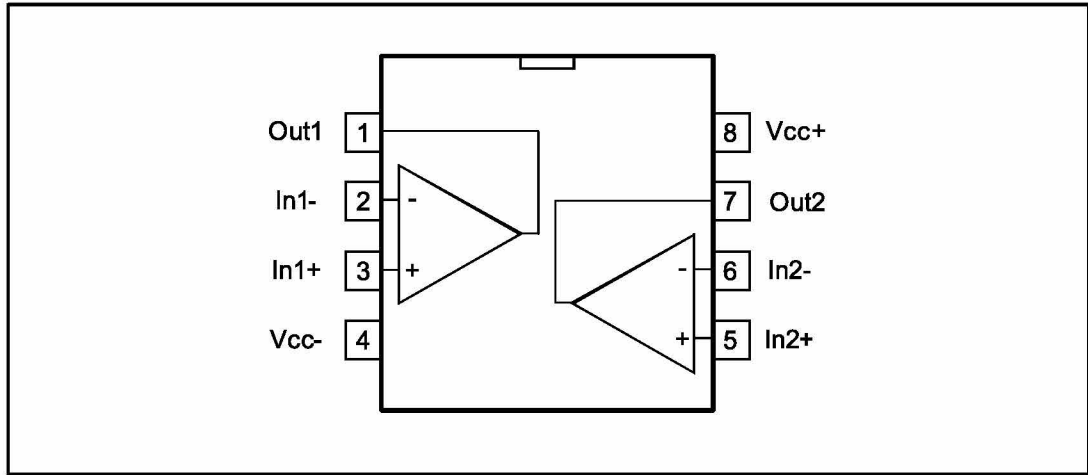


Table 2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOIC, TSSOP		
IN1-	2	I	Negative input
IN1+	3	I	Positive input
IN2-	6	I	Negative input
IN2+	5	I	Positive input
OUT1	1	O	Output
OUT2	7	O	Output
V <sub>CC-</sub>	4	—	Negative (lowest) supply or ground (for single-supply operation)
NC	—	—	No internal connection
V <sub>CC+</sub>	8	—	Positive (highest) supply

## 4 Absolute maximum ratings

**Table 3: Absolute maximum ratings**

Symbol	Parameter	LM158,A	LM258,A	LM358,A	Unit
V <sub>CC</sub>	Supply voltage	±16 or 32			V
V <sub>i</sub>	Input voltage	-0.3 to 32			
V <sub>id</sub>	Differential input voltage	±32			
	Output short-circuit duration <sup>(1)</sup>	Infinite			
I <sub>in</sub>	Input current <sup>(2)</sup>	5 mA in DC or 50 mA in AC (duty cycle = 10 %, T = 1 s)			mA
T <sub>oper</sub>	Operating free-air temperature range	-55 to 125	-40 to 105	0 to 70	°C
T <sub>stg</sub>	Storage temperature range	-65 to 150			
T <sub>j</sub>	Maximum junction temperature	150			
R <sub>thja</sub>	Thermal resistance junction to ambient <sup>(3)</sup>	SOIC8	125		°C/W
		TSSOP8	120		
R <sub>thjc</sub>	Thermal resistance junction to case <sup>(3)</sup>	SOIC8	40		
		TSSOP8	37		
ESD	HBM: human body model <sup>(4)</sup>	300			V
	MM: machine model <sup>(5)</sup>	200			
	CDM: charged device model <sup>(6)</sup>	1.5			kV

**Notes:**

<sup>(1)</sup>Short-circuits from the output to V<sub>CC</sub> can cause excessive heating if V<sub>CC</sub> > 15 V. The maximum output current is approximately 40 mA independent of the magnitude of V<sub>CC</sub>. Destructive dissipation can result from simultaneous short circuits on all amplifiers.

<sup>(2)</sup>This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V<sub>CC</sub> voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.

<sup>(3)</sup>Short-circuits can cause excessive heating and destructive dissipation. R<sub>th</sub> are typical values.

<sup>(4)</sup>Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

<sup>(5)</sup>Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

<sup>(6)</sup>Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

**Table 4: Operating conditions**

Symbol	Parameter		Value	Unit
$V_{CC}$	Supply voltage		3 to 30	V
$V_{icm}$	Common mode input voltage range $T_{amb} = 25^{\circ}\text{C}$ <sup>(1)</sup>		$(V_{CC-})$ to $(V_{CC+} - 1.5)$	
	Common mode input voltage range $(T_{min} \leq T_{amb} \leq T_{max})$ <sup>(2)</sup>		$(V_{CC-})$ to $(V_{CC+} - 2)$	
$T_{oper}$	Operating free air temperature range	LM158	-55 to 125	°C
		LM258	-20 to 85	
		LM358	0 to 70	

**Notes:**

<sup>(1)</sup>When used in comparator, the functionality is guaranteed as long as at least one input remains within the operating common mode voltage range.

<sup>(2)</sup>When used in comparator, the functionality is guaranteed as long as at least one input remains within the operating common mode voltage range.

## 5 Electrical characteristics

Table 5: Electrical characteristics for  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = \text{Ground}$ ,  $V_o = 1.4\text{ V}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$   
(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	
$V_{io}$	Input offset voltage <sup>(1)</sup>	LM158A		2	mV	
		LM258A, LM358A		2		
		LM158		5		
		LM358, LM258		3		
	$T_{min} \leq T_{amb} \leq T_{max}$	LM158A, LM258A, LM358A		4		
		LM158, LM258		7		
LM358			9			
$\Delta V_{io}/\Delta T$	Input offset voltage drift	LM158A, LM258A, LM358A	7	15	$\mu\text{V}/^\circ\text{C}$	
		LM158, LM258, LM358	7	30		
$I_{io}$	Input offset current	LM158A, LM258A, LM358A	2	10	nA	
		LM158, LM258, LM358	2	30		
	$T_{min} \leq T_{amb} \leq T_{max}$	LM158A, LM258A, LM358A		30		
		LM158, LM258, LM358		40		
$\Delta I_{io}/\Delta T$	Input offset current drift	LM158A, LM258A, LM358A	10	200	$\text{pA}/^\circ\text{C}$	
		LM158, LM258, LM358	10	300		
$I_{ib}$	Input bias current <sup>(2)</sup>	LM158A, LM258A, LM358A	20	50	nA	
		LM158, LM258, LM358	20	150		
	$T_{min} \leq T_{amb} \leq T_{max}$	LM158A, LM258A, LM358A		100		
		LM158, LM258, LM358		200		
$A_{vd}$	Large signal voltage gain	$V_{CC+} = 15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_o = 1.4\text{ V to } 11.4\text{ V}$	50	100	V/mV	
		$T_{min} \leq T_{amb} \leq T_{max}$	25			
SVR	Supply voltage rejection ratio	$V_{CC+} = 5\text{ V to } 30\text{ V}$ , $R_s \leq 10\text{ k}\Omega$	65	100	dB	
		$T_{min} \leq T_{amb} \leq T_{max}$	65			
$I_{cc}$	Supply current, all amp, no load	$T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC+} = 5\text{ V}$		0.7	mA	
		$T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC+} = 30\text{ V}$		2		
CMR	Common mode rejection ratio	$R_s \leq 10\text{ k}\Omega$	70	85	dB	
		$T_{min} \leq T_{amb} \leq T_{max}$	60			
$I_{source}$	Output current source	$V_{CC+} = 15\text{ V}$ , $V_o = 2\text{ V}$ , $V_{id} = 1\text{ V}$	20	40	60	mA
$I_{sink}$	Output sink current	$V_{CC+} = 15\text{ V}$ , $V_o = 2\text{ V}$ , $V_{id} = -1\text{ V}$	10	20		mA
		$V_{CC+} = 15\text{ V}$ , $V_o = 0.2\text{ V}$ , $V_{id} = -1\text{ V}$	12	50		$\mu\text{A}$

Symbol	Parameter	Min.	Typ.	Max.	Unit	
V <sub>OH</sub>	High level output voltage	V <sub>CC+</sub> = 30 V, R <sub>L</sub> = 2 kΩ connected to V <sub>CC-</sub> , T <sub>amb</sub> = 25 °C	26	27		V
		V <sub>CC+</sub> = 30 V, R <sub>L</sub> = 2 kΩ connected to V <sub>CC-</sub> , T <sub>min</sub> ≤ T <sub>amb</sub> ≤ T <sub>max</sub>	26			
		V <sub>CC+</sub> = 30 V, R <sub>L</sub> = 10 kΩ connected to V <sub>CC-</sub> , T <sub>amb</sub> = 25 °C	27	28		
		V <sub>CC+</sub> = 30 V, R <sub>L</sub> = 10 kΩ connected to V <sub>CC-</sub> , T <sub>min</sub> ≤ T <sub>amb</sub> ≤ T <sub>max</sub>	27			
		V <sub>CC+</sub> = 5 V, R <sub>L</sub> = 2 kΩ connected to V <sub>CC-</sub> , T <sub>amb</sub> = 25 °C	3.5			
		V <sub>CC+</sub> = 5 V, R <sub>L</sub> = 2 kΩ connected to V <sub>CC-</sub> , T <sub>min</sub> ≤ T <sub>amb</sub> ≤ T <sub>max</sub>	3			
V <sub>OL</sub>	Low level output voltage	R <sub>L</sub> = 10 kΩ connected to V <sub>CC-</sub>		5	20	mV
		T <sub>min</sub> ≤ T <sub>amb</sub> ≤ T <sub>max</sub>			20	
SR	Slew rate	V <sub>CC+</sub> = 15 V, V <sub>i</sub> = 0.5 to 3 V, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, unity gain				
GBP	Gain bandwidth product	V <sub>CC+</sub> = 30 V, f = 100 kHz, V <sub>in</sub> = 10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF				
THD	Total harmonic distortion	f = 1 kHz, A <sub>v</sub> = 20 dB, R <sub>L</sub> = 2 kΩ, V <sub>o</sub> = 2 V <sub>pp</sub> , C <sub>L</sub> = 100 pF, V <sub>o</sub> = 2 V <sub>pp</sub>				
e <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz, R <sub>s</sub> = 100 Ω, V <sub>CC+</sub> = 30 V				
V <sub>o1</sub> /V <sub>o2</sub>	Channel separation <sup>(3)</sup>	1 kHz ≤ f ≤ 20 kHz				

**Notes:**

<sup>(1)</sup>V<sub>o</sub> = 1.4 V, R<sub>s</sub> = 0 Ω, 5 V < V<sub>CC+</sub> < 30 V, 0 < V<sub>ic</sub> < V<sub>CC+</sub> - 1.5 V

<sup>(2)</sup>The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.

<sup>(3)</sup>Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

## 6 Electrical characteristic curves

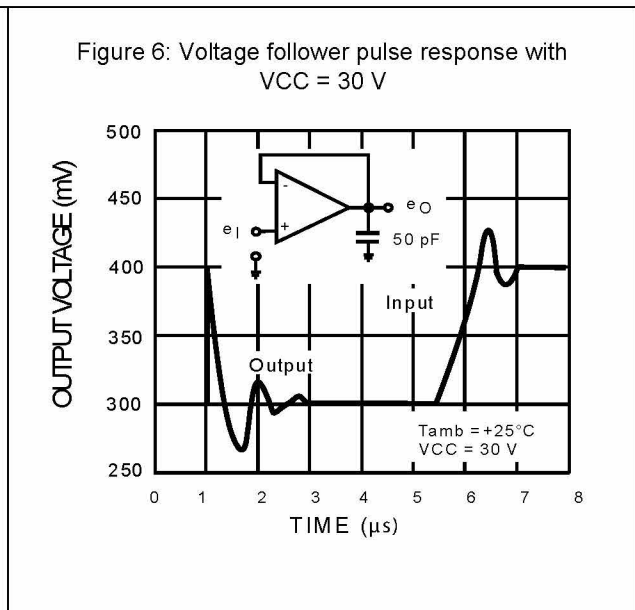
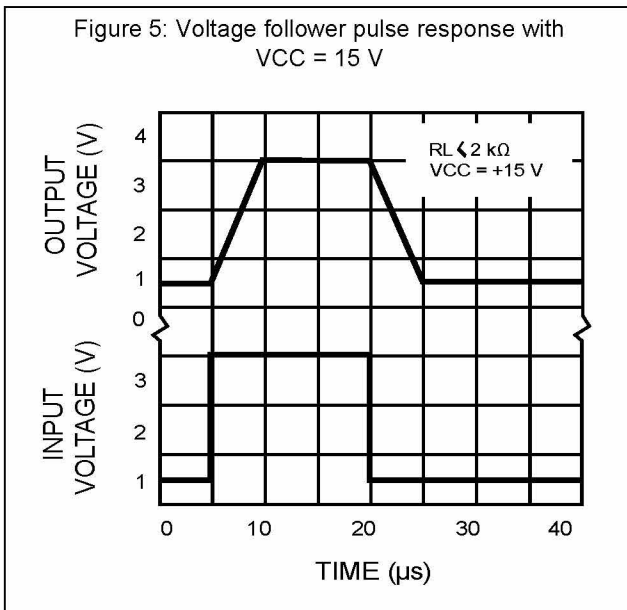
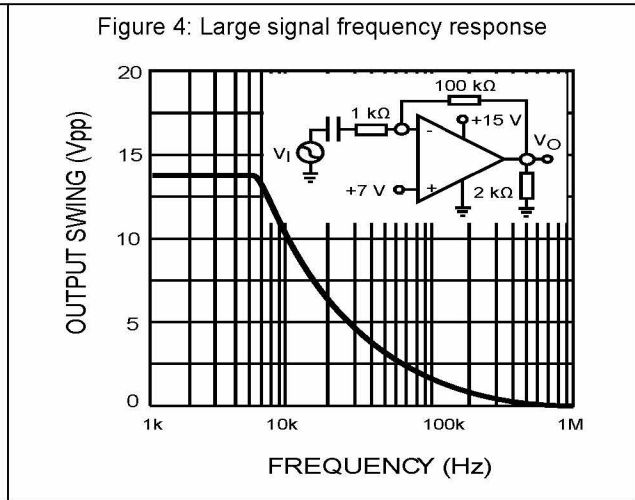
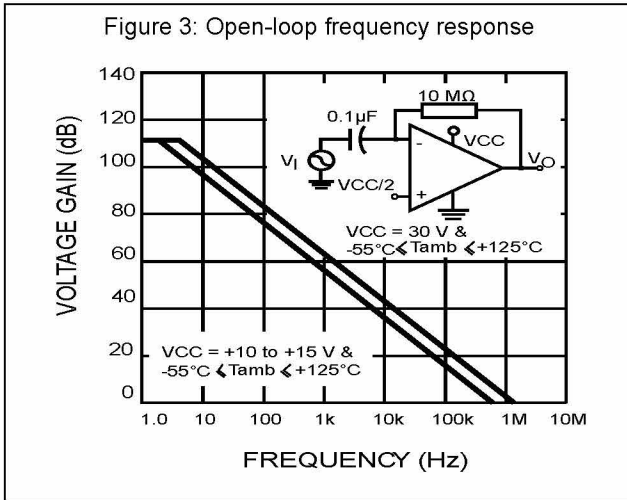




Figure 7: Input current

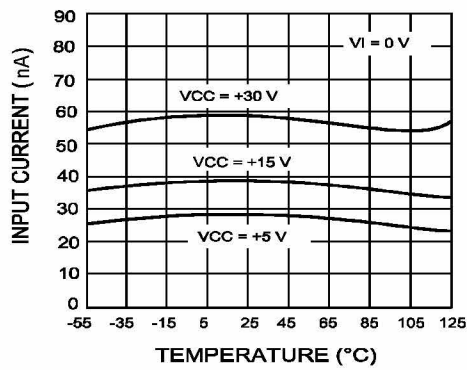


Figure 8: Output voltage vs sink current

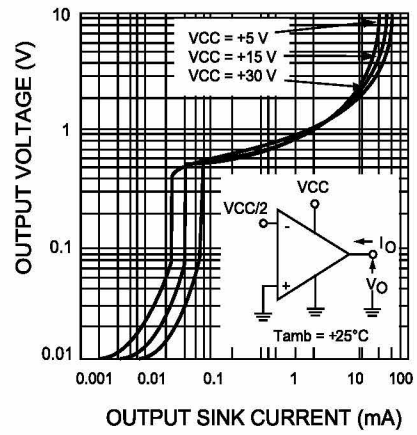


Figure 9: Output voltage vs source current

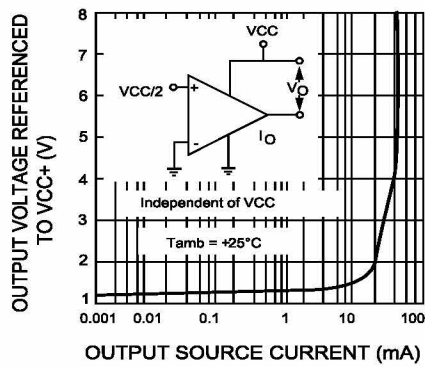


Figure 10: Current limiting

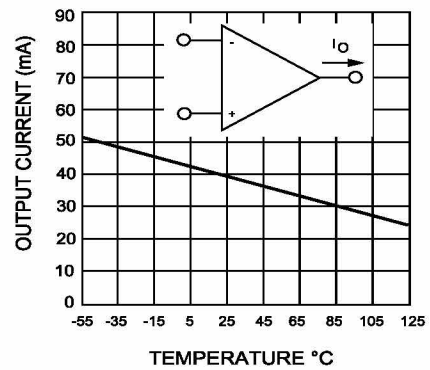


Figure 11: Input voltage range

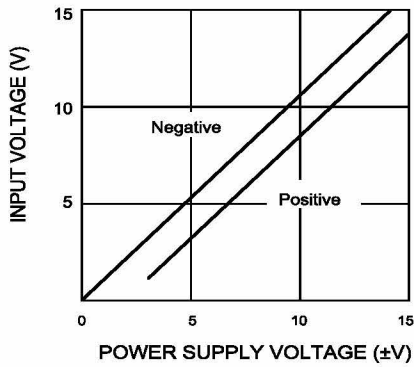


Figure 12: Open-loop gain

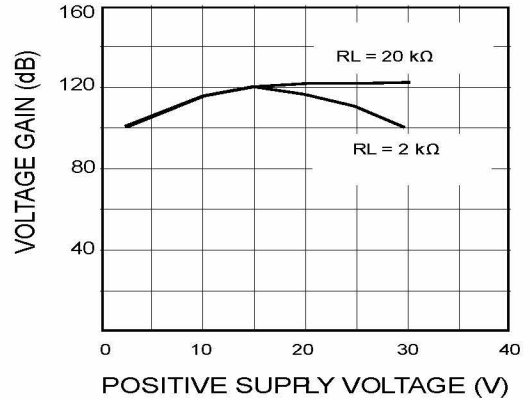


Figure 13: Supply current

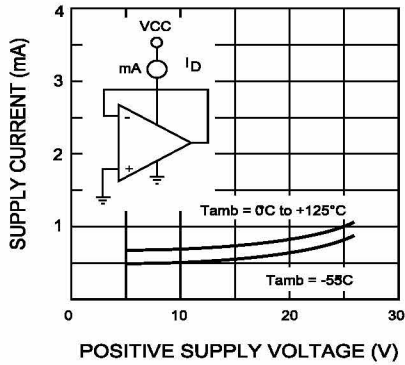


Figure 14: Input current

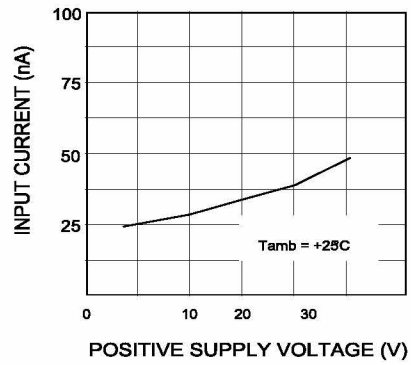


Figure 15: Gain bandwidth product

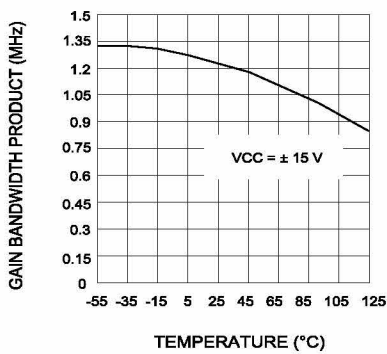


Figure 16: Power supply rejection ratio

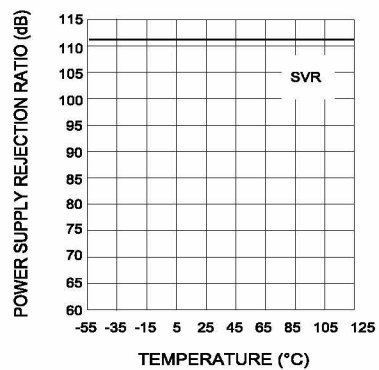


Figure 17: Common-mode rejection ratio

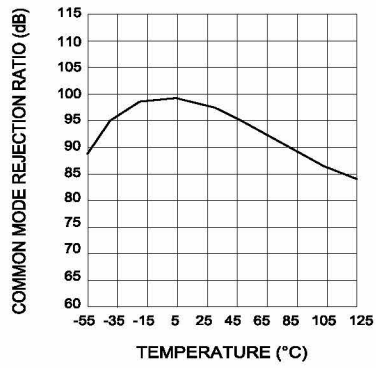
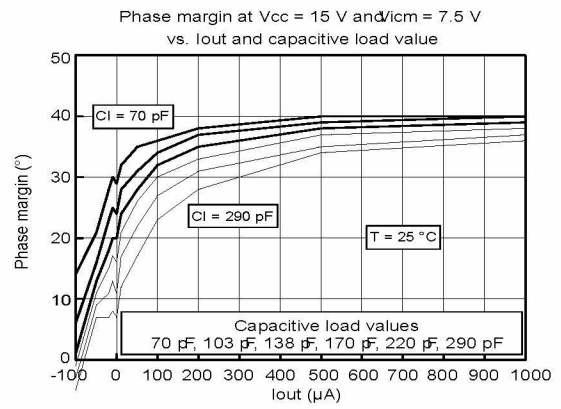


Figure 18: Phase margin vs. capacitive load



## 7 Typical applications

Single supply voltage  $V_{CC} = 5 V_{DC}$ .

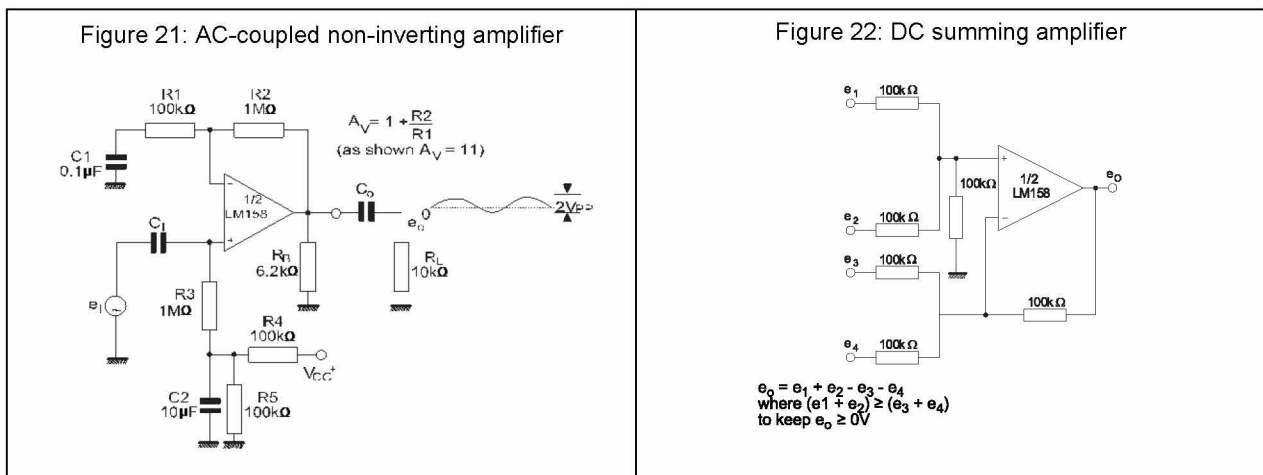
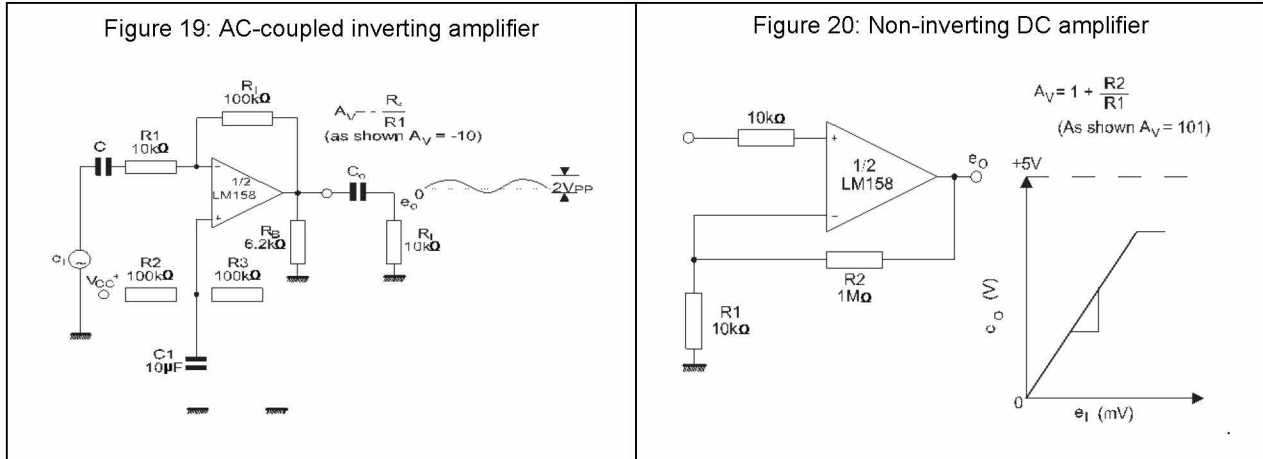
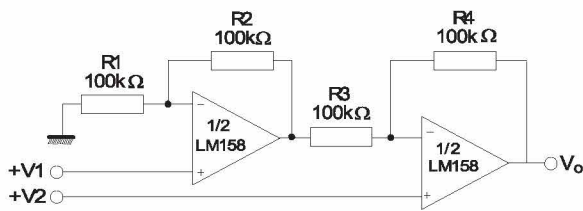
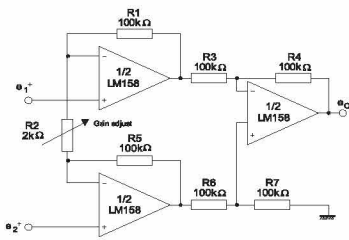


Figure 23: High input Z, DC differential amplifier



if  $R_1 = R_5$  and  $R_3 = R_4 = R_6 = R_7$   
 $e_o = [1 + \frac{2R_1}{R_2}] (e_2 + e_1)$   
 As shown  $e_o = 101 (e_2 + e_1)$

Figure 24: High input Z adjustable gain DC instrumentation amplifier



if  $R_1 = R_5$  and  $R_3 = R_4 = R_6 = R_7$   
 $e_o = [1 + \frac{2R_1}{R_2}] (e_2 + e_1)$

As shown  $e_o = 101 (e_2 + e_1)$

Figure 25: Using symmetrical amplifiers to reduce input current

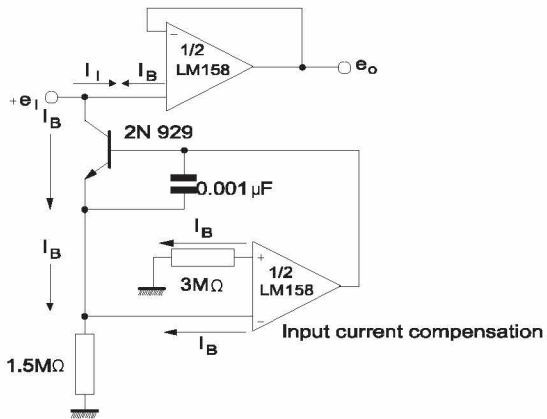
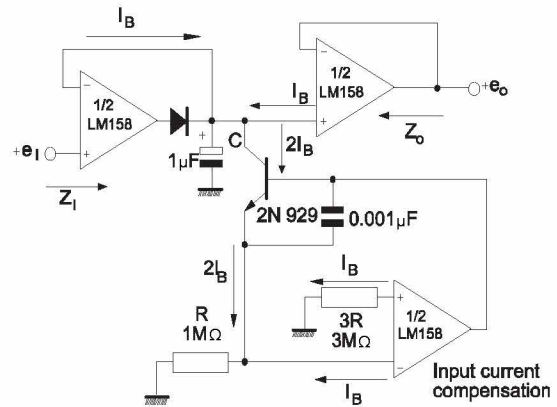
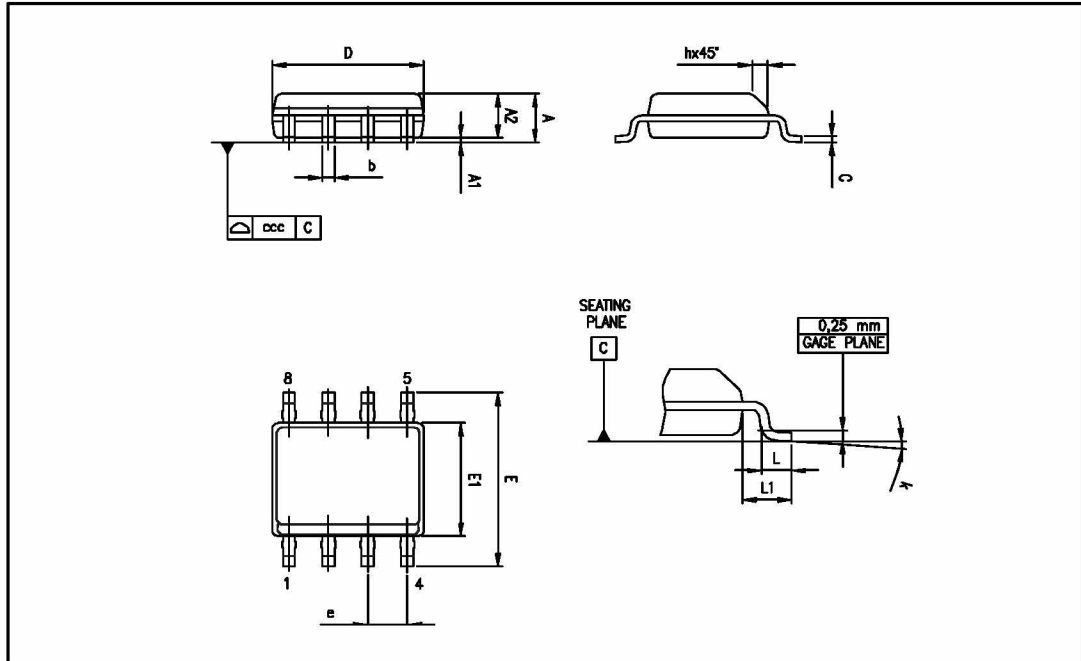
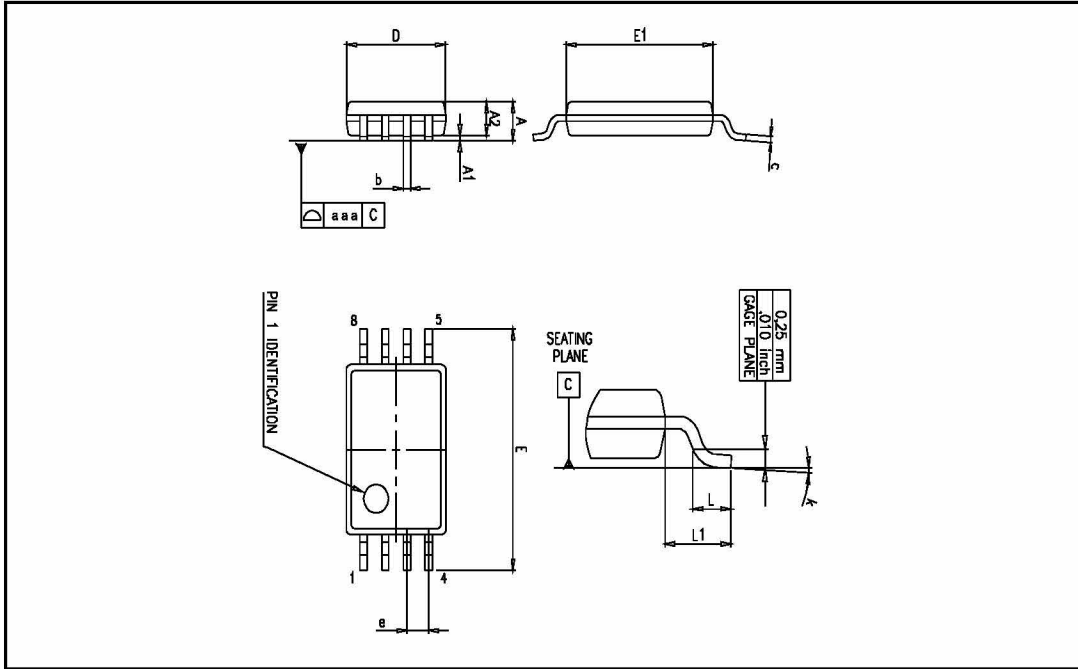


Figure 26: Low drift peak detector



**7.1 SOIC 8 package information**
**Figure 27: SOIC 8 package outline**

**Table 4: SOIC 8 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

**7.2 TSSOP8 package information**
**Figure 32: TSSOP8 package outline**

**Table 7: TSSOP8 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	