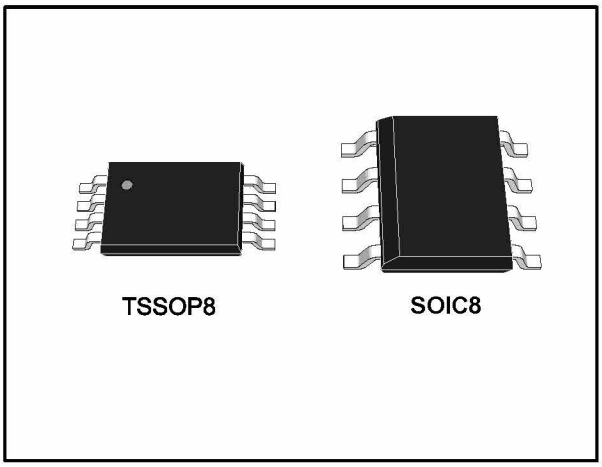
Low-power dual operational amplifiers

Description

These circuits consist of two independent, high-gain, internally frequency-compensated op amps, specifically designed to operate from a single power supply over a wide range of voltages. The low-power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard 5 V, which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.



Features

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 0.7 MHz (temperature compensated)
- Very low supply current per channel essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 3 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to (V_{CC}^+ - 1.5 V)

Applications

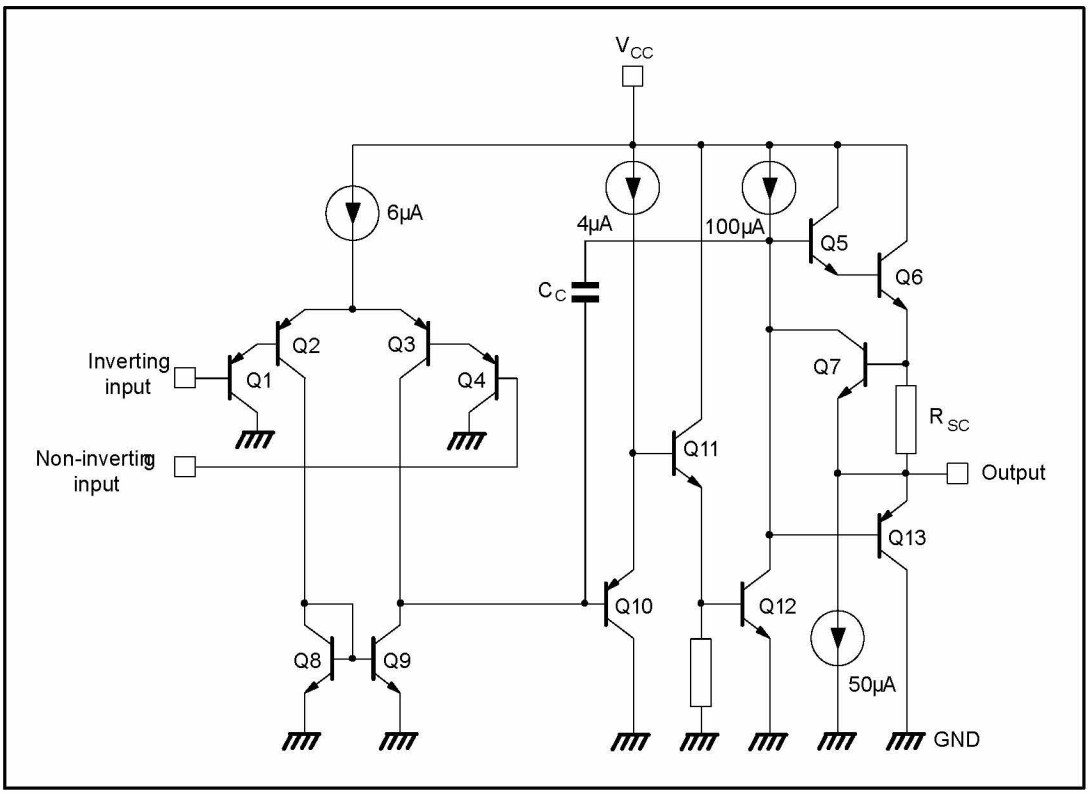
- Merchant network and server power supply units
- Multi-function printers
- Power supplies and mobile chargers
- Motor control: AC induction, brushed DC
- Desktop PC and motherboard
- Indoor and outdoor air conditioners
- Washers, dryers, and refrigerators
- AC inverters, string inverters, central inverters, and voltage frequency drives
- Uninterruptible power supplies
- Electronic point-of-sale systems

1 Ordering information Table 1.

Part Number	Package	Packing	Temperature(TA)	Package Qty	ESD protection
LM2904DR	SOIC-8	Reel	-40°C ~ 125°C	2500	300V
LM2904PWR	TSSOP-8	Reel	-40°C ~ 125°C	2500	300V
LM2904AVQDR	SOIC-8	Reel	-40°C ~ 125°C	2500	2000V
LM2904AVQPWR	TSSOP-8	Reel	-40°C ~ 125°C	2500	2000V

2 Schematic diagram

Figure 1: Schematic diagram (1/2 LM2904)



3 Package pin connections

Figure 2: Pin connections (top view)

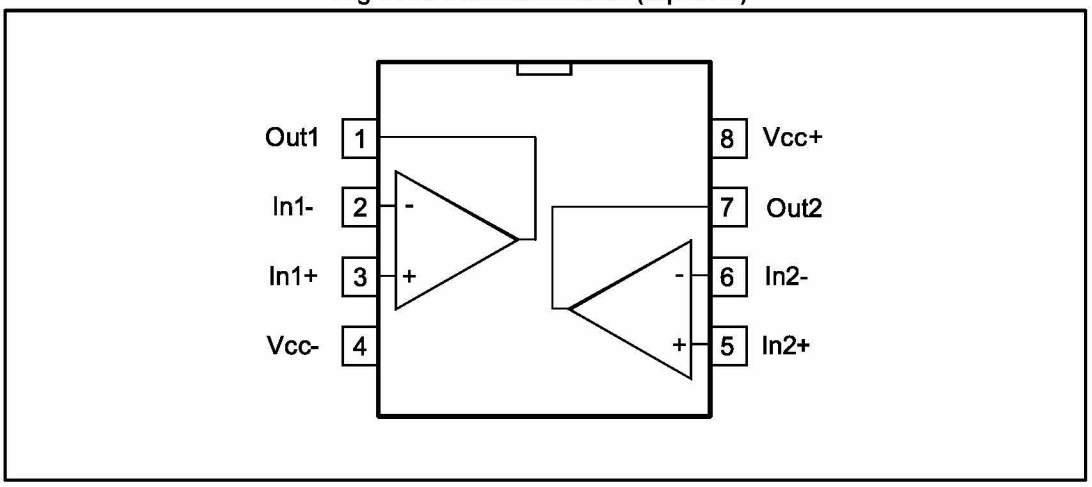


Table 2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOIC, TSSOP		
IN1–	2	I	Negative input
IN1+	3	I	Positive input
IN2–	6	I	Negative input
IN2+	5	I	Positive input
OUT1	1	O	Output
OUT2	7	O	Output
V_{CC}–	4	—	Negative (lowest) supply or ground (for single-supply operation)
NC	—	—	No internal connection
V_{CC}+	8	—	Positive (highest) supply

4 Absolute maximum ratings and operating conditions Table 3.

Symbol	Parameter		LM2904	LM2904,A	Unit
V_{CC}	Supply voltage		±16 or 32		V
V_i	Input voltage		-0.3 to 32		
V_{id}	Differential input voltage		±32		
	Output short-circuit duration (1)		Infinite		
I_{in}	Input current (2)		5 mA in DC or 50 mA in AC (duty cycle = 10 %, T = 1 s)		mA
T_{oper}	Operating free-air temperature range			-40 to 125	°C
T_{stg}	Storage temperature range		-65 to 150		
T_j	Maximum junction temperature		150		
R_{thja}	Thermal resistance junction to ambient (3)	SOIC8	125		°C/W
		TSSOP8	120		
R_{thjc}	Thermal resistance junction to case (3)	SOIC8	40		
		TSSOP8	37		
ESD	HBM: human body model (4)		300		V
	MM: machine model (5)		200		
	CDM: charged device model (6)		1.5		kV

1. *All voltage values, except differential voltage are with respect to network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.*
3. *Short-circuits from the output to V_{CC} can cause excessive heating if (V_{cc}^+) > 15 V. The maximum output current is approximately 40 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.*
4. *This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as an input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.*
5. *The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400 µA max ($R = (V_{in} - 32\ V)/400\ \mu A$).*
6. *Short-circuits can cause excessive heating and destructive dissipation. Values are typical.*

   Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

   Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

4 Absolute maximum ratings and operating conditions

SR	unity gain, T_{amb} = 25 °C				V/µs
	Slew rate, V_{CC}^+ = 15 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_L =100 pF, unity gain, $T_{min} \le T_{amb} \le T_{max}$	0.2			
GBP	Gain bandwidth product, f = 100 kHz, V_{CC}^+ = 30 V, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF	0.7	1.1		MHz
THD	Total harmonic distortion, f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_{CC}^+ = 30 V		0.02		%
e_n	Equivalent input noise voltage, f = 1 kHz, R_S = 100 Ω, V_{CC}^+ = 30 V		55		nV/√Hz
V_{O1}/V_{O2}	Channel separation, 1 kHz ≤ f ≤ 20 kHz (3)		120		dB

1. *V_O = 1.4 V, 5 V < V_{CC}^+ < 30 V, 0 V < V_{ic} < (V_{CC}^+) - 1.5 V*
2. *The direction of the input current is out of the IC. This current is essentially constant as long as the output is not saturated, so there is no change in the loading charge on the input lines.*
3. *Due to the proximity of external components, ensure that the stray capacitance does not cause coupling between these external parts. This can typically be detected at higher frequencies because this type of capacitance increases.*

4.1 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S= ([V+] – [V–])	LM2904	3	30	V
		LM2904V	3	26	
V_{CM}	Common-mode voltage		V–	V+ – 2	V
T_A	Operating ambient temperature	LM2904, LM2904V	–40	125	°C

5 Electrical characteristics

Table 4. V_{CC}^+ = 5 V, V_{CC}- = ground, V_O = 1.4 V, R_L connected to GND, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage, T_{amb} = 25 °C, LM2904		3	7	mV
	Input offset voltage, T_{amb} = 25 °C, LM2904A		1	2	
	Input offset voltage, $T_{min} \le T_{amb} \le T_{max}$, LM2904			9	
	Input offset voltage, $T_{min} \le T_{amb} \le T_{max}$, LM2904A			4	
$\Delta V_{io}/\Delta T$	Input offset voltage drift		7	30	µV/°C
I_{io}	Input offset current, T_{amb} = 25 °C		2	30	nA
	Input offset current, $T_{min} \le T_{amb} \le T_{max}$			40	
$\Delta I_{io}/\Delta T$	Input offset current drift		10	300	pA/°C
I_{ib}	Input bias current, T_{amb} = 25 °C (2)		20	150	nA
	Input bias current, $T_{min} \le T_{amb} \le T_{max}$ (2)			200	
A_{vd}	Large signal voltage gain, V_{CC}^+ = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V, T_{amb} = 25 °C	50	100		V/mV
	Large signal voltage gain, V_{CC}^+ = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V, $T_{min} \le T_{amb} \le T_{max}$	25			
SVR	Supply voltage rejection ratio, V_{CC}^+ = 5 V to 30 V, V_{icm} = 0 V, T_{amb} = 25 °C	65	100		dB
	Supply voltage rejection ratio, V_{CC}^+ = 5 V to 30 V, V_{icm} = 0 V, $T_{min} \le T_{amb} \le T_{max}$	65			
I_{CC}	Supply current, all amp, no load, T_{amb} = 25 °C, V_{CC}^+ = 5 V		0.7	1.2	mA
	Supply current, all amp, no load, $T_{min} \le T_{amb} \le T_{max}$, V_{CC}^+ = 30 V			2	
CMR	Common-mode rejection ratio, V_{CC}^+ = 30 V, V_{icm} = 0 V to 28.5 V, T_{amb} = 25 °C	70	85		dB
	Common-mode rejection ratio, V_{CC}^+ = 30 V, V_{icm} = 0 V to 28 V, $T_{min} \le T_{amb} \le T_{max}$	60			
I_{source}	Output short-circuit current, V_{CC}^+ = 15 V, V_o = 2 V, V_{id} = 1 V	20	40	60	mA
I_{sink}	Output sink current, V_O = 2 V, V_{CC+} = 15 V	10	20		
	Output sink current, V_O = 0.2 V, V_{CC+} = 15 V	12	50		µA

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage	V_{CC}+ = 30 V, R_L = 2 kΩ connected to V_{CC}-, T_{amb} = 25 °C	26	27		V
		V_{CC}+ = 30 V, R_L = 2 kΩ connected to V_{CC}-, $T_{min} \le T_{amb} \le T_{max}$	26			
		V_{CC}+ = 30 V, R_L = 10 kΩ connected to V_{CC}-, T_{amb} = 25 °C	27	28		
		V_{CC}+ = 30 V, R_L = 10 kΩ connected to V_{CC}-, $T_{min} \le T_{amb} \le T_{max}$	27			
		V_{CC}+ = 5 V, R_L = 2 kΩ connected to V_{CC}-, T_{amb} = 25 °C	3.5			
		V_{CC}+ = 5 V, R_L = 2 kΩ connected to V_{CC}-, $T_{min} \le T_{amb} \le T_{max}$	3			
V_{OL}	Low level output voltage	R_L = 10 kΩ connected to V_{CC}-		5	20	mV
		$T_{min} \le T_{amb} \le T_{max}$			20	
SR	Slew rate	V_{CC}^+ = 15 V, V_i = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain		0.3	0.6	V/μs
GBP	Gain bandwidth product	V_{CC}^+ = 30 V, f = 100 kHz, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF		0.7	1.1	MHz
THD	Total harmonic distortion	f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_O = 2 V_{pp}		0.02		%
e_n	Equivalent input noise voltage	f = 1 kHz, R_s = 100 Ω, V_{CC}^+ = 30 V		55		
V_{o1}/V_{o2}	Channel separation (3)	1 kHz ≤ f ≤ 20 kHz		120		dB

Notes:

(1) V_o = 1.4 V, R_s = 0 Ω, 5 V < V_{CC}^+ < 30 V, 0 < V_{ic} < V_{CC}^+ - 1.5 V

(2) The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.

(3) Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

6 Electrical characteristic curves

Figure 3: Open-loop frequency response

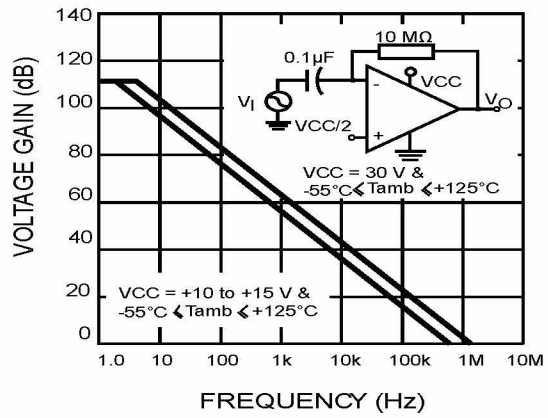


Figure 4: Large signal frequency response

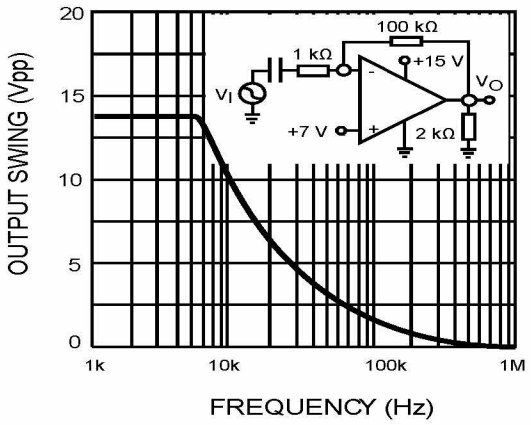


Figure 5: Voltage follower pulse response with VCC = 15 V

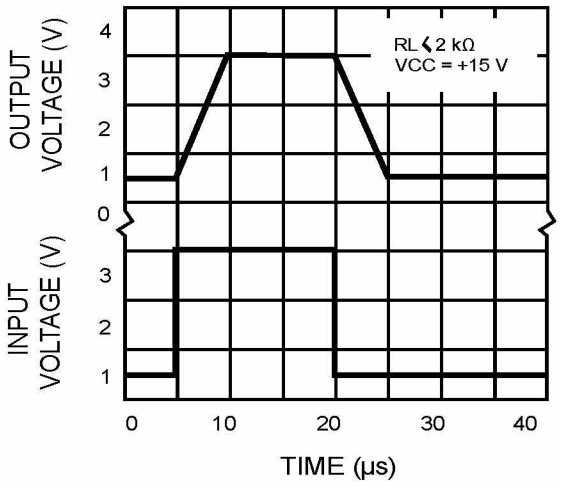


Figure 6: Voltage follower pulse response with VCC = 30 V

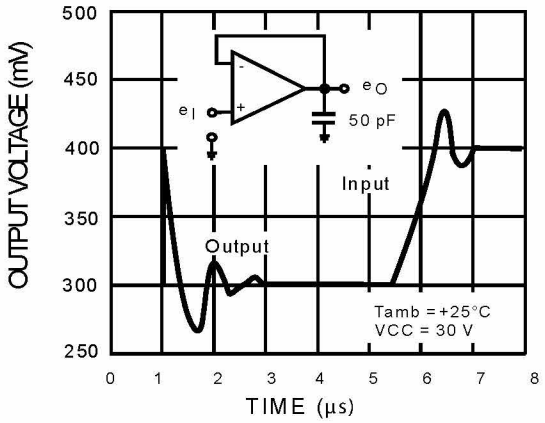


Figure 7: Input current

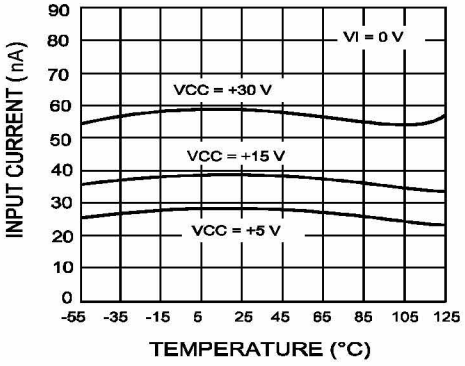


Figure 8: Output voltage vs sink current

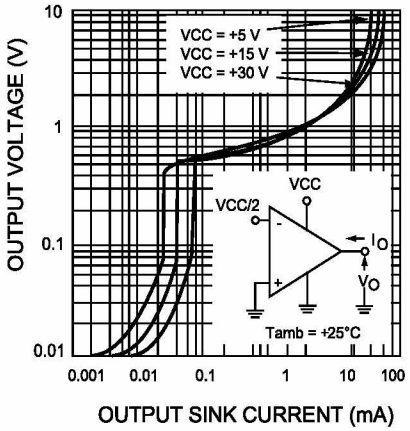


Figure 9: Output voltage vs source current

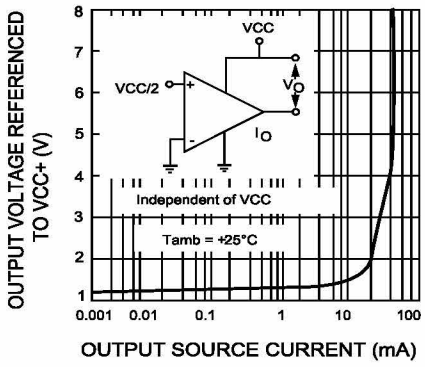


Figure 10: Current limiting

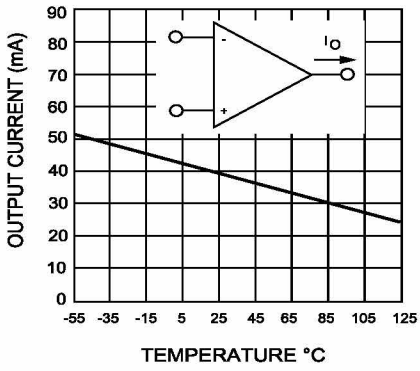


Figure 11: Input voltage range

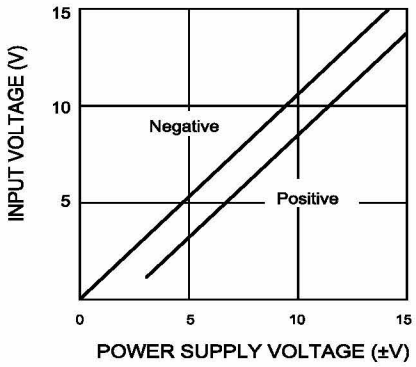


Figure 12: Open-loop gain

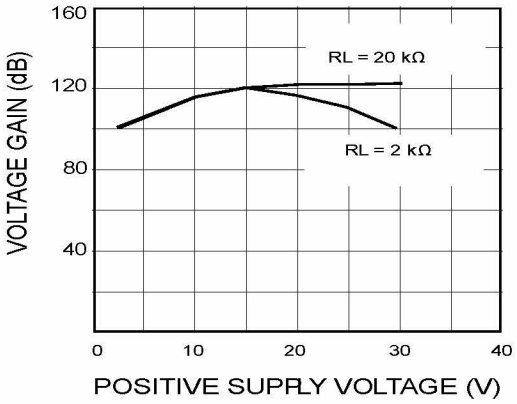


Figure 13: Supply current

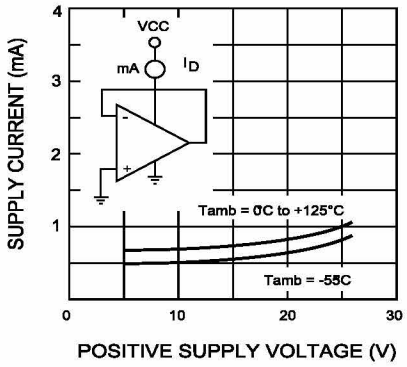


Figure 14: Input current

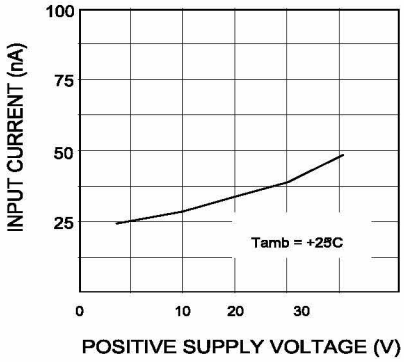


Figure 15: Gain bandwidth product

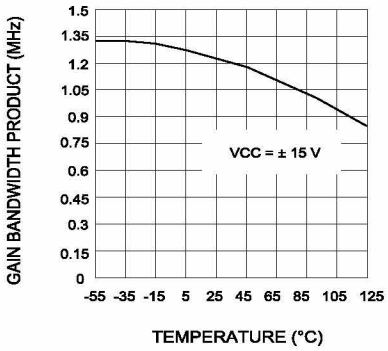


Figure 16: Power supply rejection ratio

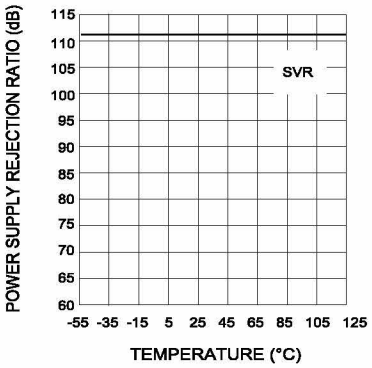


Figure 17: Common-mode rejection ratio

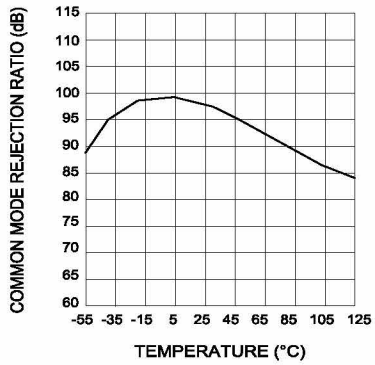
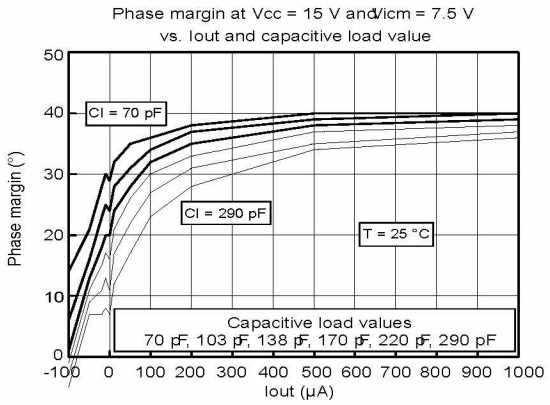


Figure 18: Phase margin vs. capacitive load



7 Typical applications

Single supply voltage V_{CC} = 5 V_{DC}.

Figure 19: AC-coupled inverting amplifier

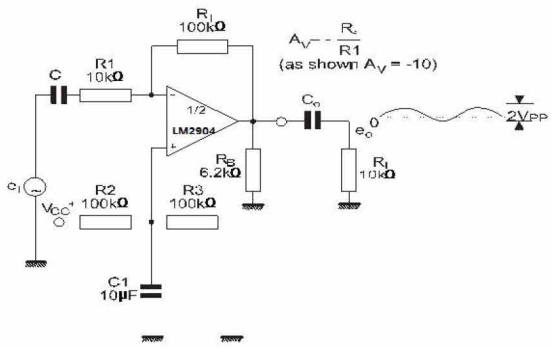


Figure 20: Non-inverting DC amplifier

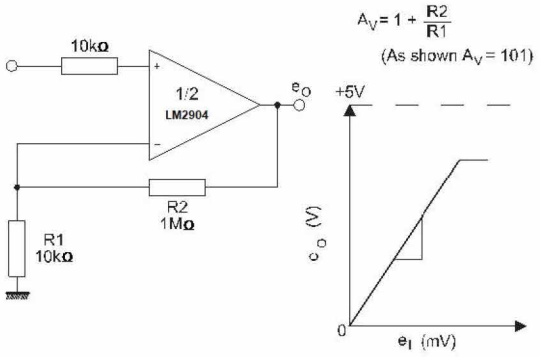


Figure 21: AC-coupled non-inverting amplifier

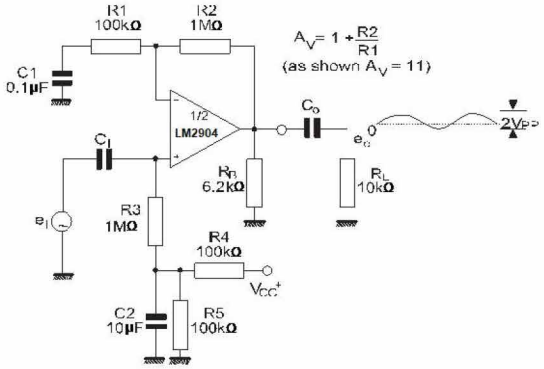
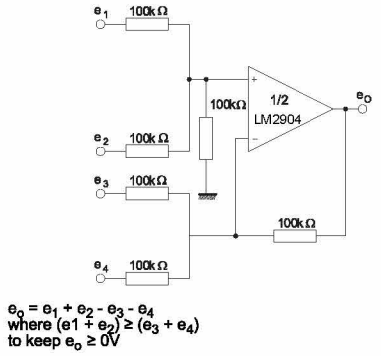
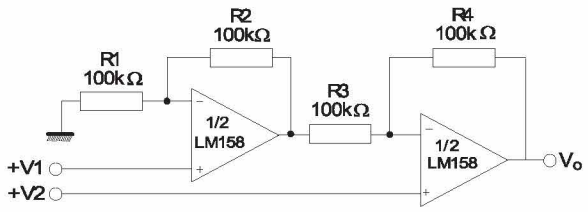


Figure 22: DC summing amplifier



$e_o = e_1 + e_2 - e_3 - e_4$
where $(e1 + e_2) \geq (e_3 + e_4)$
to keep $e_o \geq 0V$

Figure 23: High input Z, DC differential amplifier

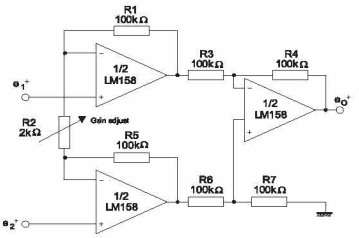


if R1 = R5 and R3 = R4 = R6 = R7

$e_o = [1 + \frac{2R1}{R2}] ((e_2 + e_1)$

As shown $e_o = 101 (e_2 + e_1)$

Figure 24: High input Z adjustable gain DC instrumentation amplifier



if R1 = R5 and
R3 = R4 = R6 = R7

$e_o = [1 + \frac{2R1}{R2}] ((e_2 + e_1)$

As shown $e_o = 101 (e_2 + e_1)$

Figure 25: Using symmetrical amplifiers to reduce input current

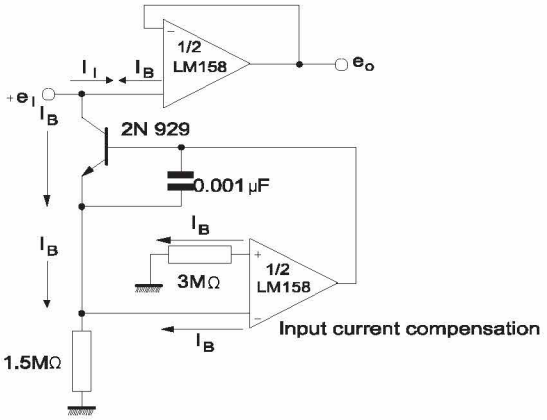
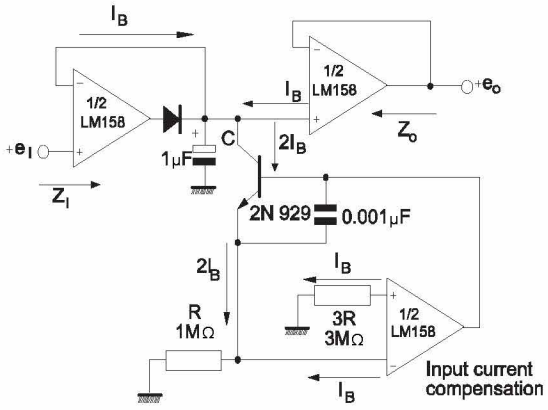


Figure 26: Low drift peak detector



7.1 SO8 package information

Figure 27: SOIC 8 package outline

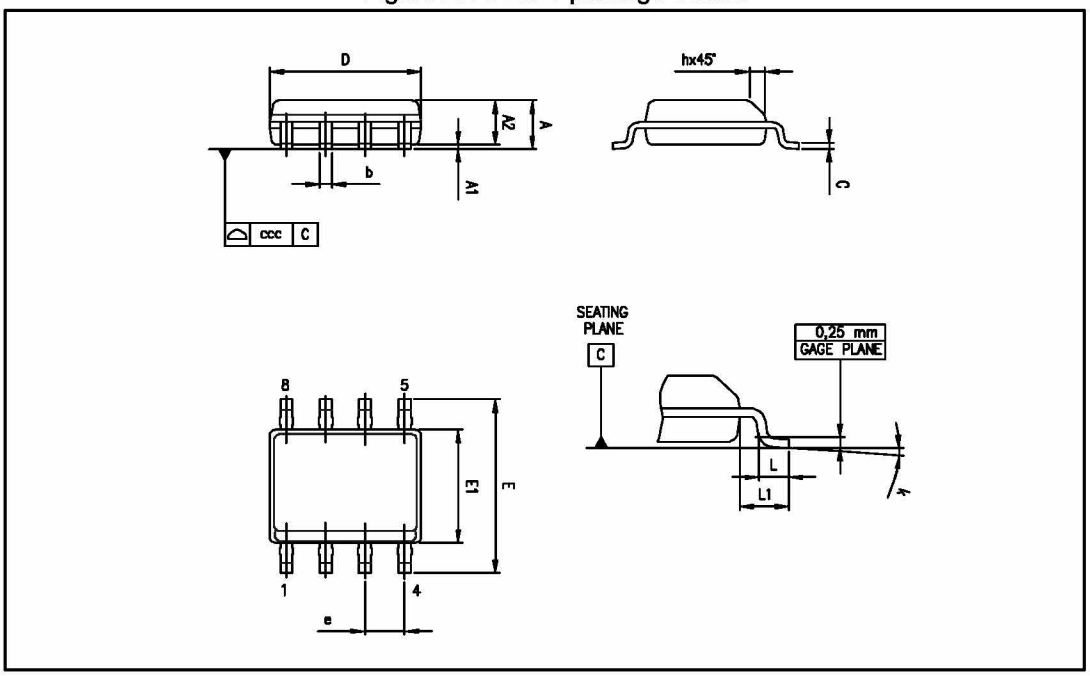


Table 4: SOIC 8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

7.2 TSSOP8 package information

Figure 28: TSSOP8 package outline

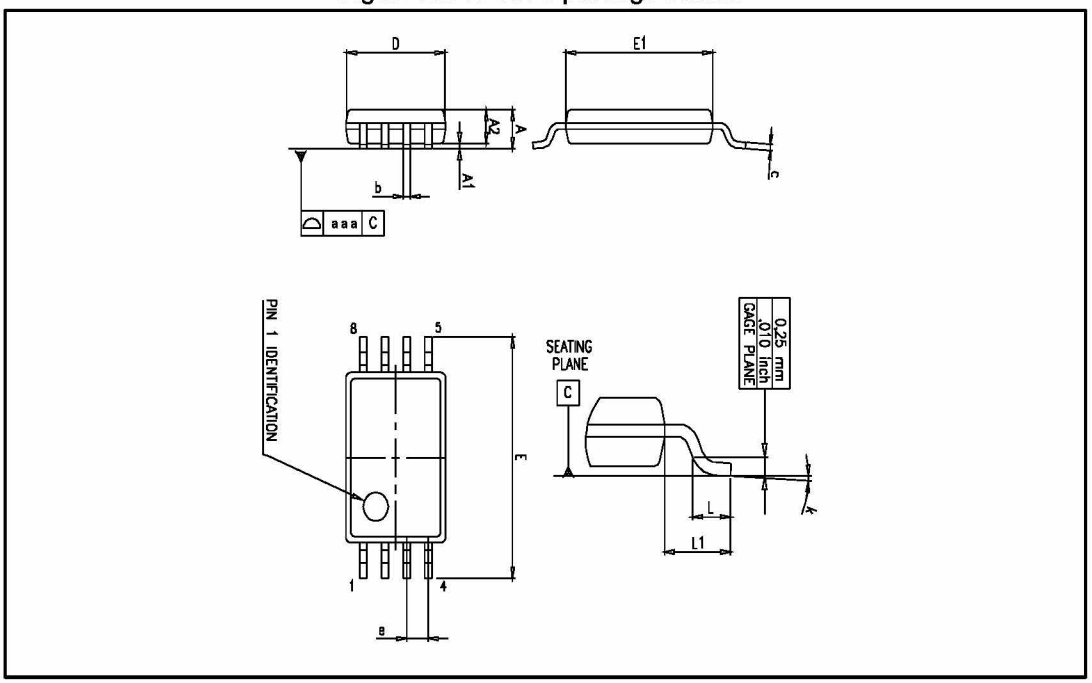


Table 7: TSSOP8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	