Low Power Quad Operational Amplifier

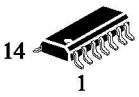
Description

The LM224/LM324 contains four independent high gain operational amplifiers with internal frequency compensation. The four op-amps operate over a wide voltage range from a single power supply. Also use a split power supply. The device has low power supply current drain, regardless of the power supply voltage. The low power drain also makes the LM224/LM324 a good choice for battery operation.

When your project calls for a traditional op-amp function, now you can streamline your design with a simple single power supply. Use ordinary +5VDC common to practically any digital system or personal computer application, without requiring an extra 15V power supply just to have the interface electronics you need.

The LM224/LM324 is a versatile, rugged workhorse with a thousand-and-one uses, from amplifying signals from a variety of transducers to dc gain blocks, or any op-amp function. The attached pages offer some recipes that will have your project cooking in no time.

P SUFFIX
TSSOP



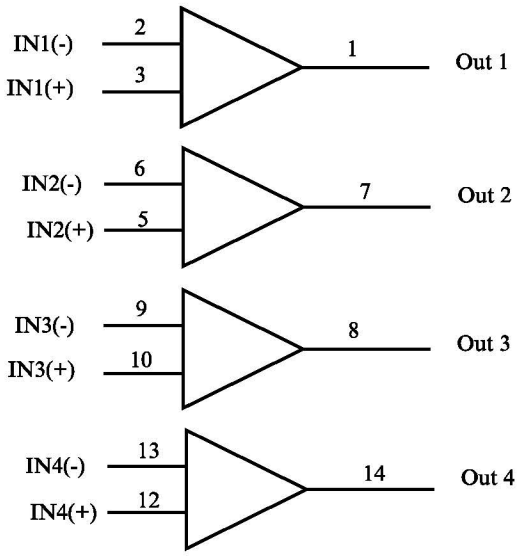
D SUFFIX
SOIC

PACKGAE INFORMATION
LM324P TSSOP
LM324D SOIC
LM224D SOIC

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range:
  3V ~ 32V (or ±1.5V ~ ±16V)
- Input common-mode voltage range includes ground
- Large output voltage swing: 0V DC to V_{CC}-1.5V DC
- Power drain suitable for battery operation
- Low input offset voltage and offset current
- Differential input voltage range equal to the power supply voltage
- Operating Temperature LM324 T_A = 0° to +70° C
- Operating Temperature LM224 T_A = -25° to +85° C

LOGIC DIAGRAM

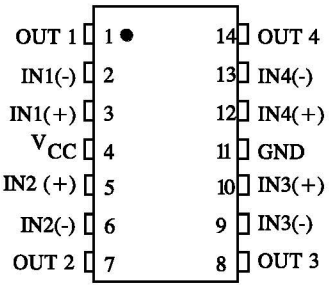


PIN 4 = V_{CC}
PIN 11= GND

Ordering information

Part Number	Package	Packing	Temperature（T_A）	Package Qty	V_{IO}
LM224DR	SOIC-14	Reel	0°C~70°C	2500	3 mV
LM224ADR	SOIC-14	Reel	0°C~70°C	2500	2 mV
LM324DR	SOIC-14	Reel	-25°C~85°C	2500	3 mV
LM324PWR	TSSOP-14	Reel	-25°C~85°C	2500	3 mV
LM324ADR	SOIC-14	Reel	-25°C~85°C	2500	2 mV
LM324APWR	TSSOP-14	Reel	-25°C~85°C	2500	2 mV

PIN ASSIGNMENT



Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOIC, TSSOP		
IN1–	2	I	Negative input
IN1+	3	I	Positive input
OUT 1	1	O	Output
IN2–	6	I	Negative input
IN2+	5	I	Positive input
OUT2	7	O	Output
IN3–	9	I	Negative input
IN3+	10	I	Positive input
OUT3	8	O	Output
IN4–	13	I	Negative input
IN4+	12	I	Positive input
OUT4	14	O	Output
V_{CC-}	11	—	Negative (lowest) supply or ground (for single-supply operation)
NC	—	—	Do not connect
V_{CC+}	4	—	Positive (highest) supply

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltages Single Supply Split Supplies	 32 ±16	V
V_{IDR}	Input Differential Voltage Range (1)	±32	V
V_{ICR}	Input Common Mode Voltage Range	-0.3 to 32	V
I_{SC}	Output Short Circuit Duration	Continuous	
T_J	Junction Temperature Plastic Packages	 150	°C
Tstg	Storage Temperature Plastic Packages	 -55 to +125	°C
I_{IN}	Input Current, per pin (2)	50	mA
T_L	Lead Temperature, 1mm from Case for 10 Seconds	260	°C

** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.
These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes:
1. Split Power Supplies.
2. V_{IN}<-0.3V. This input current will only exist when voltage at any of the input leads is driven negative.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	±2.5 or 5.0	±15 or 30	V
T_A	Operating Temperature, See the Features	-25	+85	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (T_A=-40 to +105°C)

Symbol	Parameter	Test Conditions	Guaranteed Limit			Unit
			Min	Typ	Max	
V_{IO}	Maximum Input Offset Voltage	V_O=1.4V V_{CC}=5.0-30V;R_S=0Ω V_{ICM}=0V to V_{CC}-1.7V			9.0 5.0*	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Drift	R_S=0Ω, V_{CC}=30V		7.0		μV/°C
I_{IO}	Maximum Input Offset Current	V_{CC}=5.0V			150 50*	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Drift	R_S=0Ω, V_{CC}=30V		10		pA/°C
I_{IB}	Maximum Input Bias Current	V_{CC}=5.0V			500 250*	nA
V_{ICR}	Input Common Mode Voltage Range	V_{CC}=30V	0		28	V
I_{CC}	Maximum Power Supply Current	R_L=∞,V_{CC}=30V,V_0=0V R_L=∞,V_{CC}=5V,V_0=0V			3 1.2	mA
A_{VOL}	Minimum Large Signal Open-Loop Voltage Gain	V_{CC}=15V, R_L≥2KΩ	15 25*			V/mV
V_{OH}	Minimum Output High-Level Voltage Swing	V_{CC}=30V,R_L=2KΩ V_{CC}=30V,R_L=10KΩ	26 27			V
V_{OL}	Maximum Output Low-Level Voltage Swing	V_{CC}=5V,R_L=10KΩ			20	mV
CMR	Common Mode Rejection	V_{CC}=30V, R_S=10KΩ	65*			dB
PSR	Power Supply Rejection	V_{CC}=30V	65*			dB
CS	Channel Separation	f=1KHz to 20KHz,V_{CC}=30V	-120*			dB
I_{SC}	Maximum Output Short Circuit to GND	V_{CC}=5.0V			60*	mA
I_{source}	Minimum Output Source Current	V_{IN+}=1V, V_{IN-}=0V, V_{CC}=15V, V_0=0V	10			mA
I_{sink}	Minimum Output Sink Current	V_{IN+}=0V, V_{IN-}=1V, V_{CC}=15V, V_0=15V V_{IN+}=0V, V_{IN-}=1V, V_{CC}=15V, V_0=0.2V	5 10* 12*			mA μA
V_{IDR}	Differential Input Voltage Range	All V_{IN}≥GND or V-Supply (if used)			V_{CC}*	V

*=@25°C

TYPICAL PERFORMANCE CHARACTERISTICS

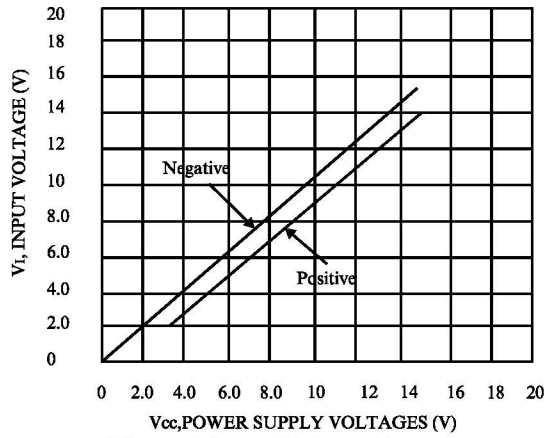


Figure 1.Input Voltage Range

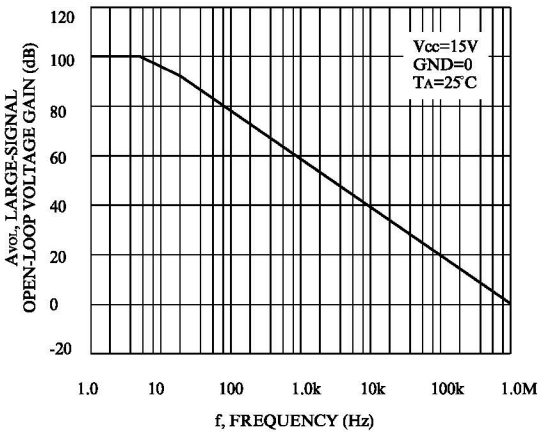


Figure 2. Open-Loop Frequency

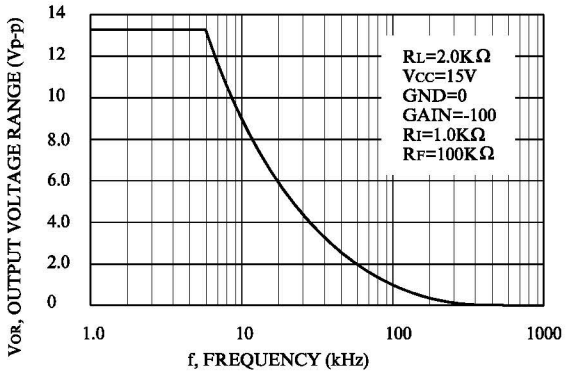


Figure 3. Large-Signal Frequency Response

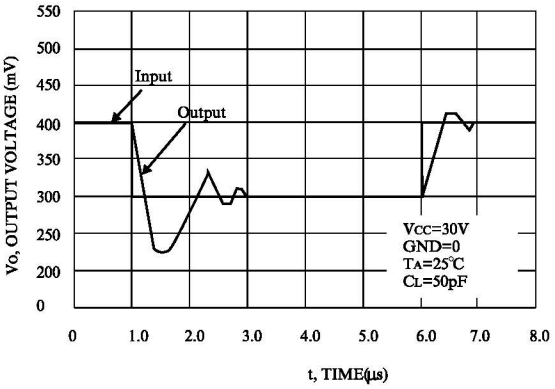


Figure 4. Small-Signal Voltage Follower Pulse Response (Noninverting)

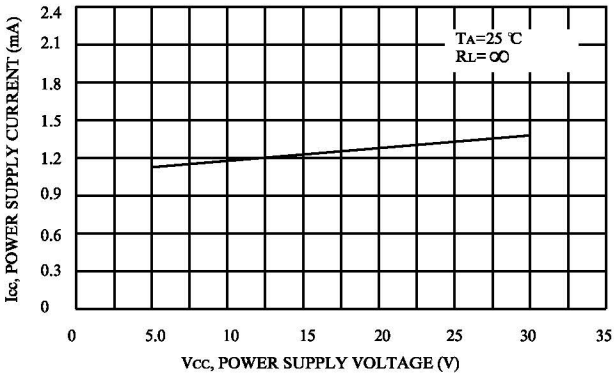


Figure 5. Power Supply Current versus Power Supply Voltage

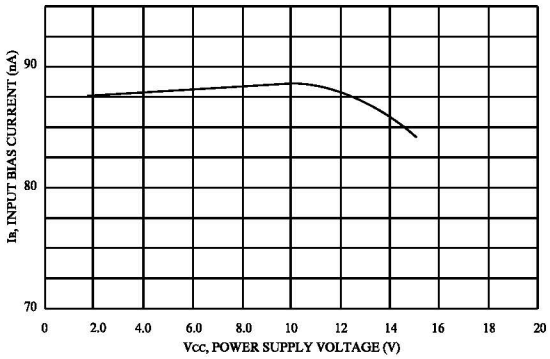


Figure 6. Input Bias Current versus Power Supply Voltage

Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

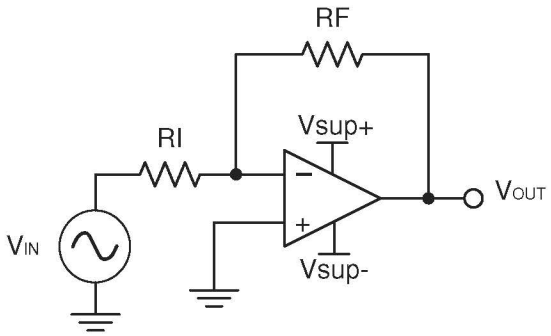
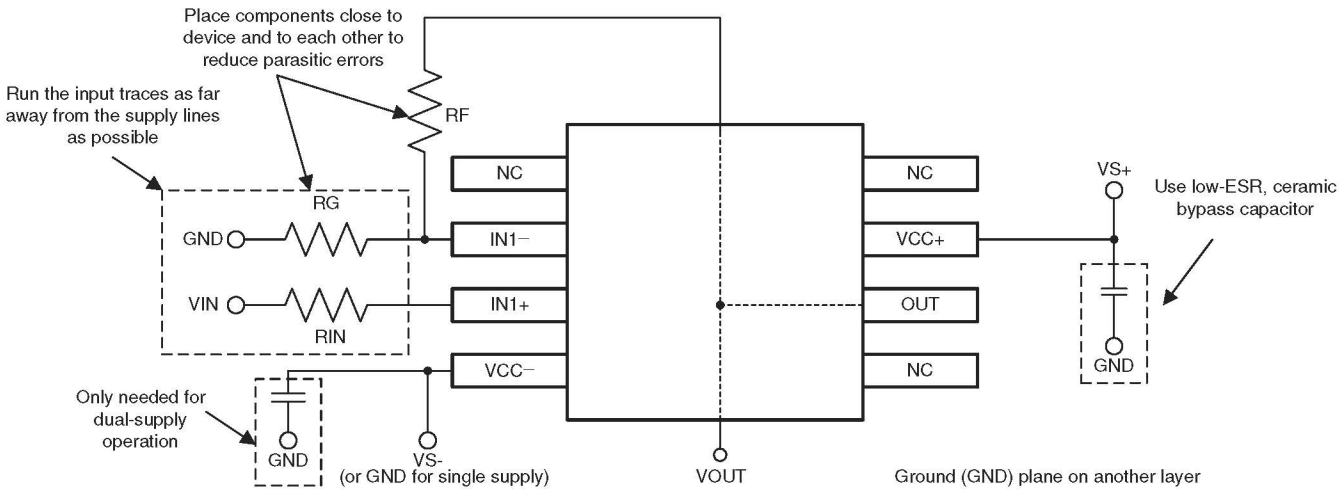


Figure 9-1. Application Schematic

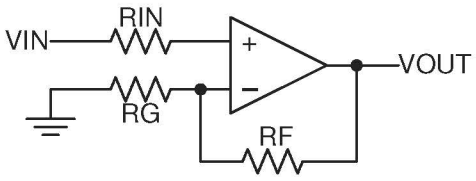
Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

Layout Examples



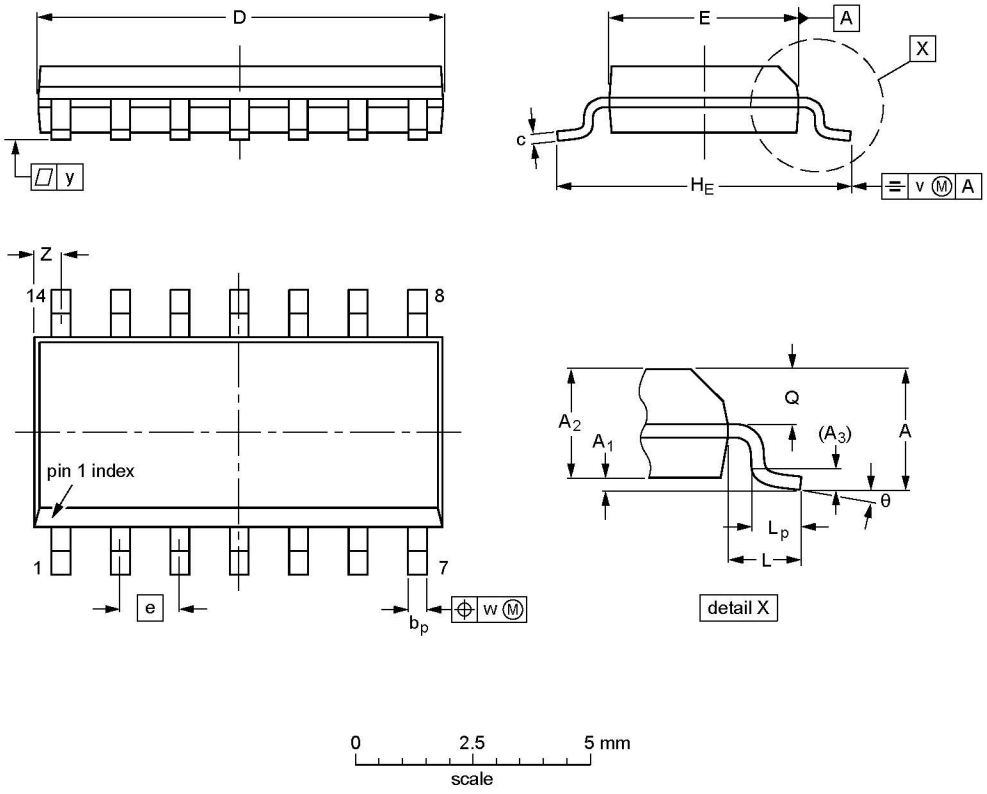
Operational Amplifier Board Layout for Noninverting Configuration



Operational Amplifier Schematic for Noninverting Configuration

Package diagram

SOIC14: plastic small outline package; 14 leads; body width 3.9 mm



DIMENSIONS (mm are the original dimensions)

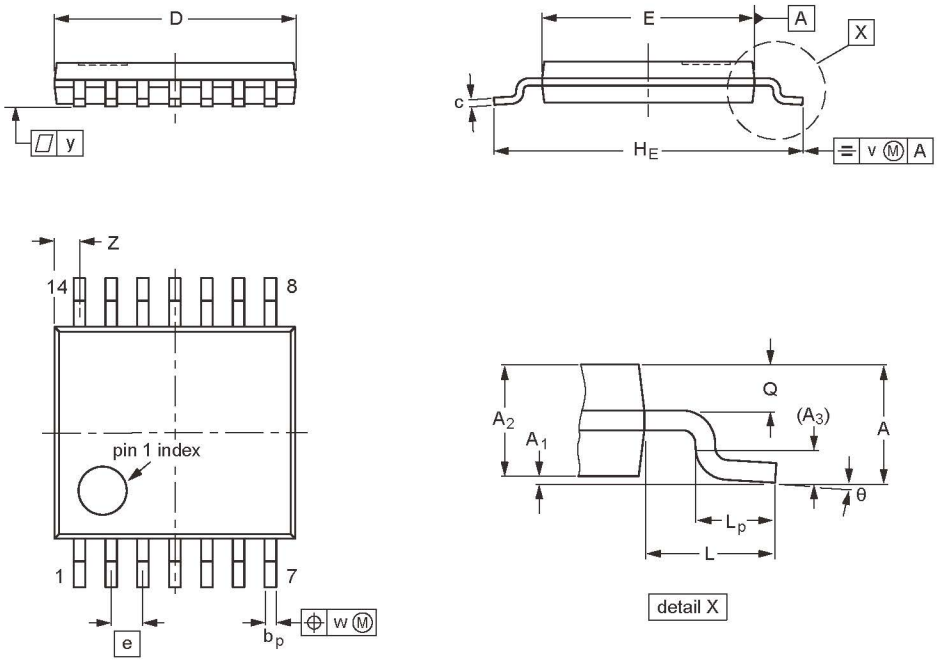
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°

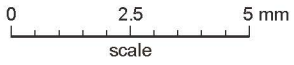
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TKSOIC14						05-06-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TKTSSOP14						05-06-19