Analog Multiplexer/Demultiplexer
High-Performance Silicon-Gate CMOS

■ DESCRIPTION

The 74HC4052 utilise silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

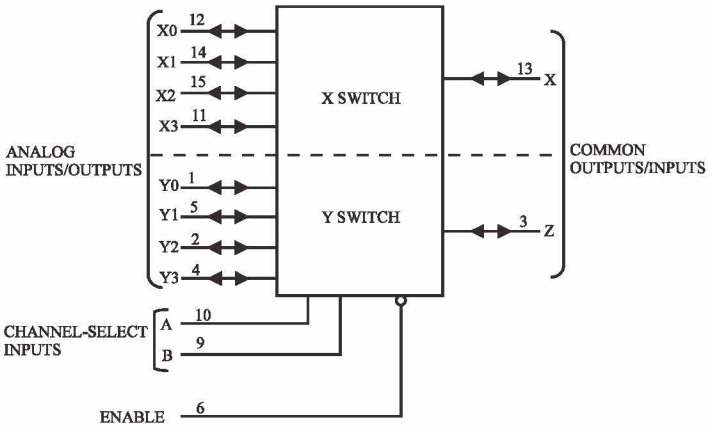
The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is high, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LS/ALS TTL outputs.

■ FEATURES

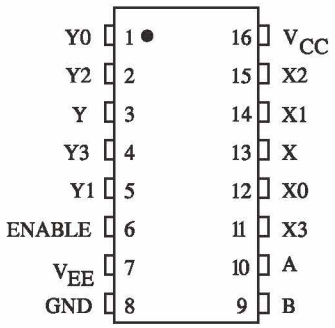
- Fast Switching and Propagation Speeds
- Digital Power Supply Range (V_{CC}-GND) = 2.0 to 6.0 V
- Analog Power Supply Range (V_{CC}-V_{EE})=2.0 to 12.0 V
- Low Crosstalk Between Switches
- TA = -40° to 125° C for all packages

■ LOGIC DIAGRAM



Double-Pole, 4-Position Plus Common Off
PIN 16 =V_{CC} PIN 7 = V_{EE} PIN 8 = GND

■ PIN ASSIGNMENT



■ FUNCTION TABLE

Control Inputs			ON Channels	
Enable	Select			
	B	A		
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	None	

H = high level L = low level X = don't care

ORDERING INFORMATION

Part Number	Package	Packing	Temperature(TA)	Package Qty
74HC4052D	SOIC-16	Reel	-40°C ~ 125°C	2500
74HC4052P	TSSOP-16	Reel	-40°C ~ 125°C	2500

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	-0.5 to +7.0 -0.5 to +14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	-7.0 to +0.5	V
V_{IS}	Analog Input Voltage	V_{EE} - 0.5 to V_{CC}+0.5	V
V_{IN}	Digital Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
I	DC Input Current Into or Out of Any Pin	±25	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SO Package+	750 500	mW
Tstg	Storage Temperature	-55 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SO Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SO Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive Supply Voltage (Referenced to GND) (Referenced to V_{EE})		2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)		- 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{IN}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		-	1.2	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Channel Select or Enable Inputs) (Figure 5)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

* For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i. e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

Part Number	Package	Packing	Temperature(TA)	Package Qty
74HC123D	SOIC-16	Reel	-40°C ~ 125°C	2500
74HC123PW	TSSOP-16	Reel	-40°C ~ 125°C	2500

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. ken to avo er than maximum rated voltages to this pper opera strained to the range indicated in the ions.. ns must be level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE}=GND, Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				-55 °C to 25°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R_{ON} = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs	R_{ON} = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I_{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V_{IN}=V_{CC} or GND, V_{EE}=-6.0 V	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V_{CC} or GND Enable = V_{CC} or GND V_{IS} = V_{CC} or GND V_{IO}= 0 V V_{EE} = GND V_{EE} = -6.0 V	 6.0 6.0	 2 8	 20 80	 40 160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					25 °C to -55°C	≤85 °C	≤125 °C	
R_{ON}	Maximum "ON" Resistance	V_{IN}=V_{IL} or V_{IH} V_{IS} = V_{CC} to V_{EE} I_S ≤ 2.0 mA	4.5 4.5 6.0	0.0 -4.5 -6.0	190 120 100	240 150 125	280 170 140	Ω
		V_{IN}=V_{IL} or V_{IH} V_{IS} = V_{CC} or V_{EE} (Endpoints) I_S ≤ 2.0 mA	4.5 4.5 6.0	0.0 -4.5 -6.0	150 100 80	190 125 100	230 140 115	
ΔR_{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V_{IN}=V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC}- V_{EE}) I_S ≤ 2.0 mA	4.5 4.5 6.0	0.0 -4.5 -6.0	30 12 10	35 15 12	40 18 14	Ω
I_{OFF}	Maximum Off- Channel Leakage Current, Any One Channel	V_{IN}=V_{IL} or V_{IH} V_{IO} = V_{CC}- V_{EE} Switch Off	6.0	-6.0	0.1	0.5	1.0	μA
	Maximum Off- Channel Leakage Current, Common Channel	V_{IN}=V_{IL} or V_{IH} V_{IO}= V_{CC}- V_{EE} Switch Off	6.0	-6.0	0.1	1.0	2.0	
I_{ON}	Maximum On- Channel Leakage Current, Channel to Channel	V_{IN}=V_{IL} or V_{IH} Switch to Switch = V_{CC}- V_{EE}	6.0	-6.0	0.1	1.0	2.0	μA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6.0 ns)

Symbol	Parameter		V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel-Select to Analog Output (Figures 1 and 2)		2.0 4.5 6.0	370 74 63	465 93 79	550 110 94	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , Analog Input to Analog Output (Figures 3 and 4)		2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay , Enable to Analog Output (Figures 5 and 6)		2.0 4.5 6.0	290 58 49	364 73 62	430 86 73	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay , Enable to Analog Output (Figures 5 and 6)		2.0 4.5 6.0	345 69 59	435 87 74	515 103 87	ns
t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	Maximum Propagation Delay, Channel-Select to Analog Input (Figures 5 and 6)		2.0 4.5 6.0	370 74 63	465 93 79	550 110 94	ns
C_{IN}	Maximum Input Capacitance, Channel-Select or Enable Inputs		-	10	10	10	pF
$C_{I/O}$	Maximum Capacitance Analog I/O	All Switches Off	-	35	35	35	pF
	Common O/I		-	80	80	80	
	Feedthrough		-	1.0	1.0	1.0	

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V, V_{EE}=0 V 80	pF

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Limit 25 °C	Unit
B_W	Maximum On-Channel Bandwidth or Minimum Frequency Response	f_{in}=1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads -3 dB R_L =50 Ω, C_L=10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	95 95 95	MHz
K_{Doff}	Off-Channel Feedthrough Isolation	f_{in} = Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L =600 Ω, C_L=50 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-50 -50 -50	dB
		f_{in} = 1.0 MHz, R_L =50 Ω, C_L=10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-40 -40 -40	
$V_{AO/I}$	Feedthrough Noise, Channel Select Input to Common O/I	f_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns) Adjust R_L at Setup so that I_S= 0 A Enable = GND R_L =600 Ω, C_L=50 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	25 105 135	mVpp
		R_L =10 Ω, C_L=10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	35 145 190	
K_{Don}	Crosstalk Between Any Two Switches	f_{in}= Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L =600 Ω, C_L=50 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-50 -50 -50	dB
		f_{in} = 1 MHz, R_L =50 Ω, C_L=10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-60 -60 -60	
THD	Total Harmonic Distortion	f_{in}= 1 kHz, R_L =10 kΩ, C_L=50 pF THD = $THD_{Measured}$ - THD_{Source} V_{IS}=4.0 V_{PP} sine wave V_{IS}=8.0 V_{PP} sine wave V_{IS}=11.0 V_{PP} sine wave	2.25 4.50 6.00	-2.25 -4.50 -6.00	0.10 0.08 0.05	%

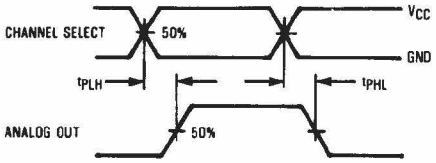
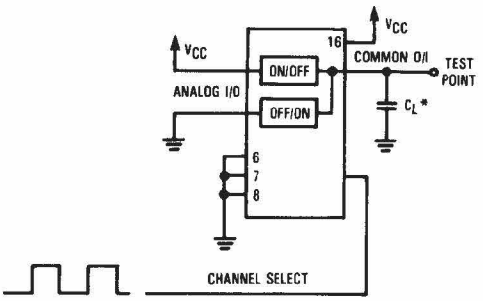


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance.

Figure 2. Test Set-UP, Channel Select to Analog Out

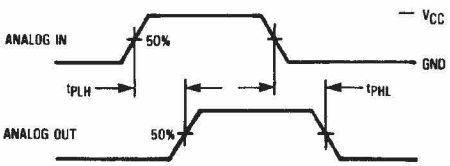
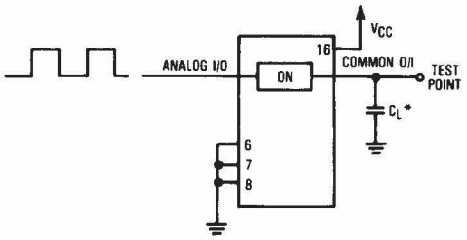


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance.

Figure 4. Test Set-UP, Analog In to Analog Out

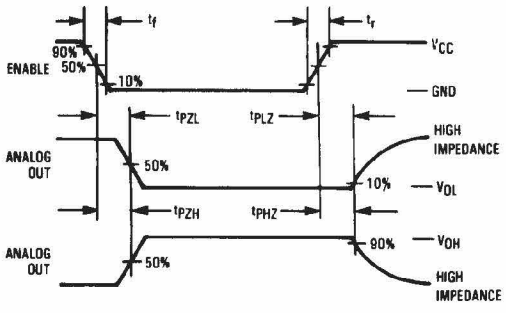


Figure 5. Switching Waveforms

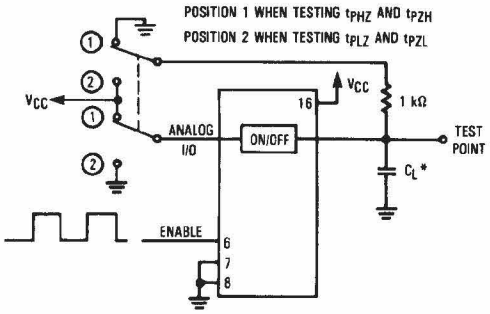
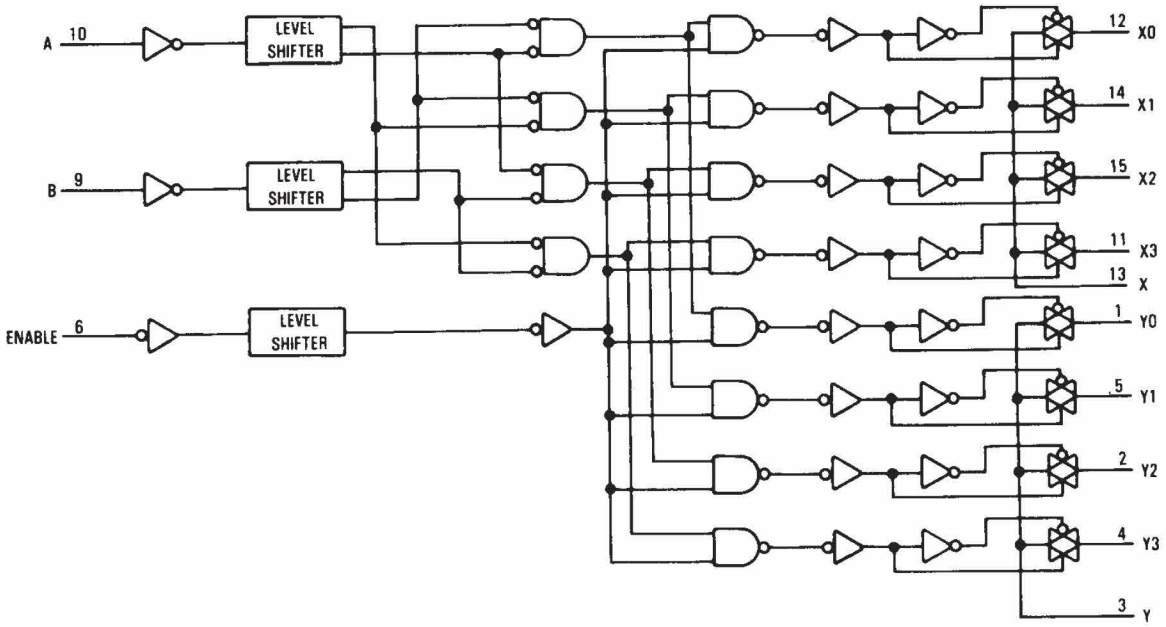
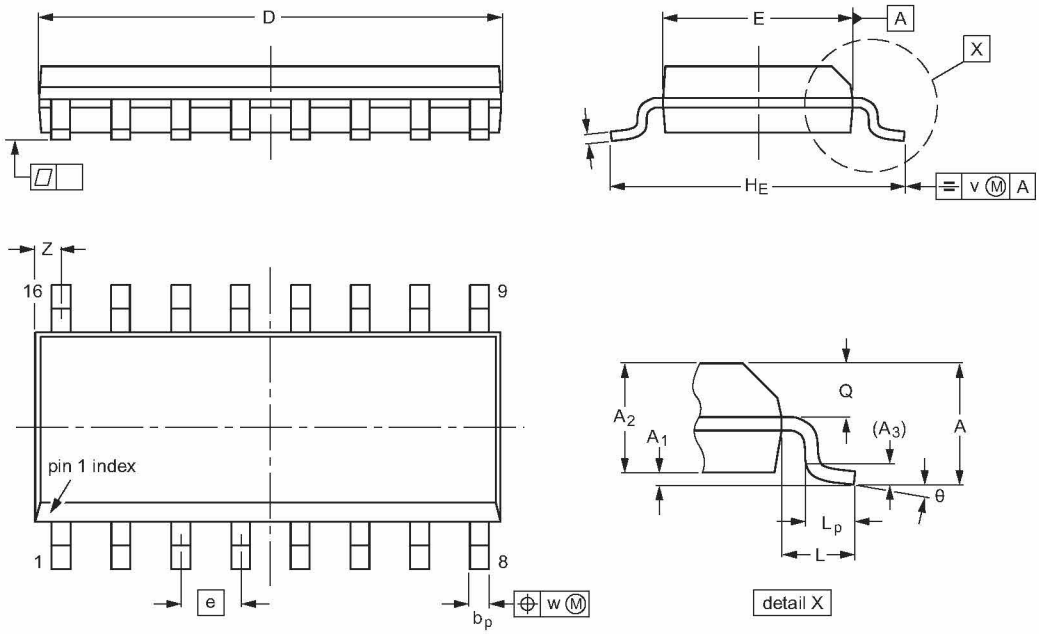


Figure 6. Test Set-UP, Enable to Analog Out

EXPANDED LOGIC DIAGRAM



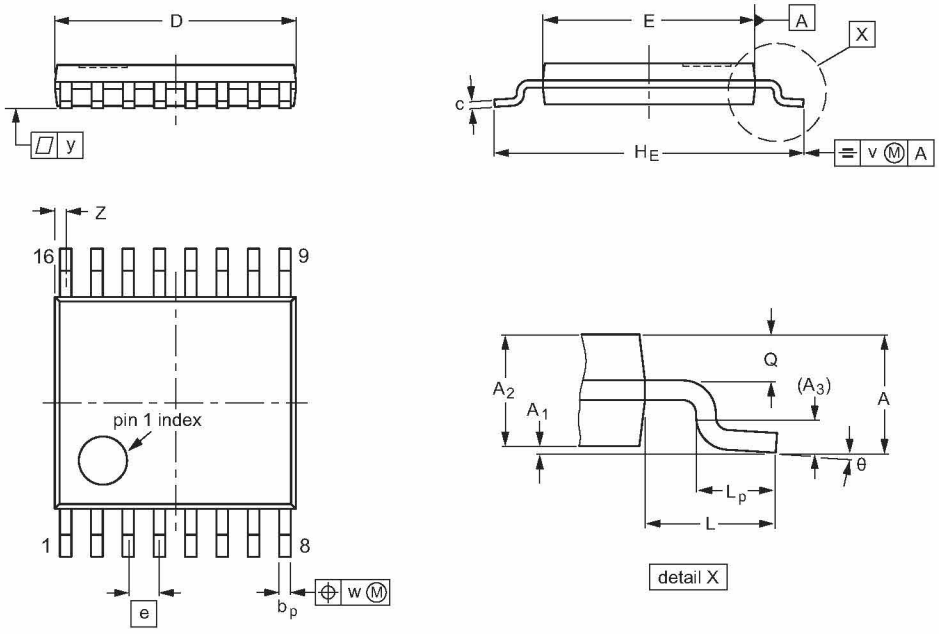
SOIC16: plastic small outline package; 16 leads; body width 3.9 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°