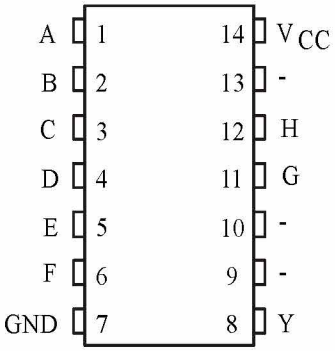
8-Input NAND Gate

■ DESCRIPTION

The 74HC30 is high-speed Si-gate CMOS device and is compatible with low power Schottky TTL (LSTTL) . The device provide the 8-input NAND function.

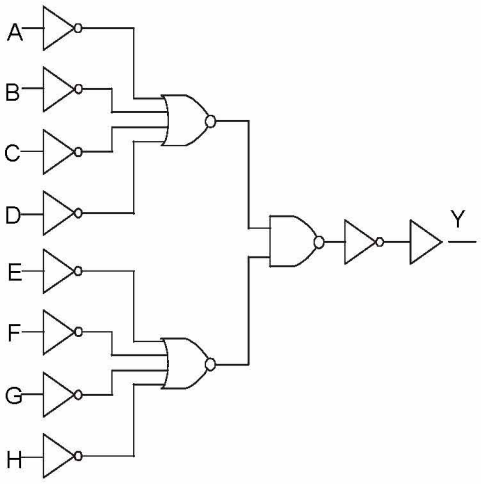
■ PIN ASSIGNMENT



■ FEATURES

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- TA = -40° to 125° C for all packages

■ LOGIC DIAGRAM



PIN 14 =V_{CC} PIN 7 = GND

■ FUNCTION TABLE

Inputs								Output
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

X = don't care

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ORDERING INFORMATION

Part Number	Package	Packing	Temperature(TA)	Package Qty
74HC30D	SOIC-14	Reel	-40°C ~ 125°C	2500
74HC30P	TSSOP-14	Reel	-40°C ~ 125°C	2500

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-55 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}≤0.1V or V_{OUT} ≥V_{CC}-0.1V $\|I_{OUT}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}≤0.1V or V_{OUT} ≥V_{CC}-0.1V $\|I_{OUT}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ - 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ - 2.4 mA	3.0	2.48	2.34	2.20	
		V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ - 4.0 mA	4.5	3.98	3.84	3.70	
		V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ - 5.2 mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 2.4 mA	3.0	0.26	0.33	0.4	
		V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 4.0 mA	4.5	0.26	0.33	0.4	
		V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 5.2 mA	6.0	0.26	0.33	0.4	
I_{IL}	Maximum Low-Level Input Leakage Current	V_{IN}= 0 V	6.0	-0.1	-1.0	-1.0	μA
I_{IH}	Maximum High-Level Input Leakage Current	V_{IN}= V_{CC}	6.0	0.1	1.0	1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or 0 V I_{OUT}=0 μA	6.0	2.0	20	40	μA

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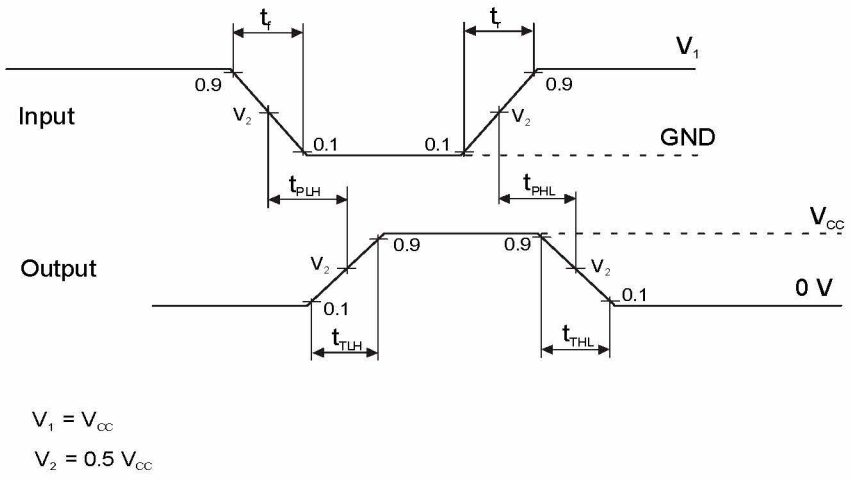
AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=6.0 ns)

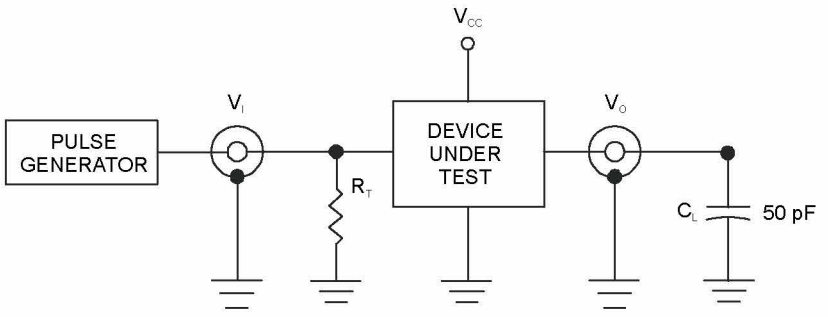
Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PHL}, t_{PLH}	Maximum Propagation Delay (Figure 1)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{THL}, t_{TLH}	Maximum Output Transition Time (Figure 1)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	5.0	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	T_A=25°C,V_{CC}=5.0 V 27	pF



$V_1 = V_{CC}$
$V_2 = 0.5\ V_{CC}$

Figure 1. Switching Waveforms



Termination resistance R_T – should be equal to Z_{OUT} of pulse generators

Figure 2. Test Circuit

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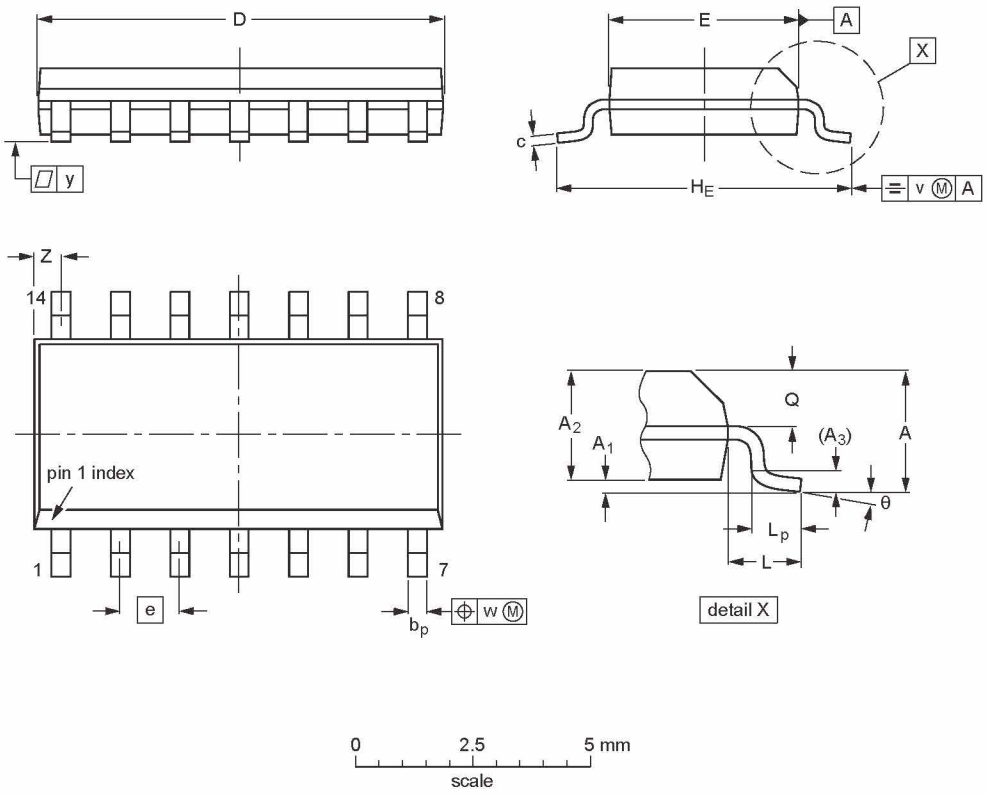
Package diagram

SOIC14: plastic small outline package; 14 leads; body width 3.9 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TKSOIC14						05-06-19

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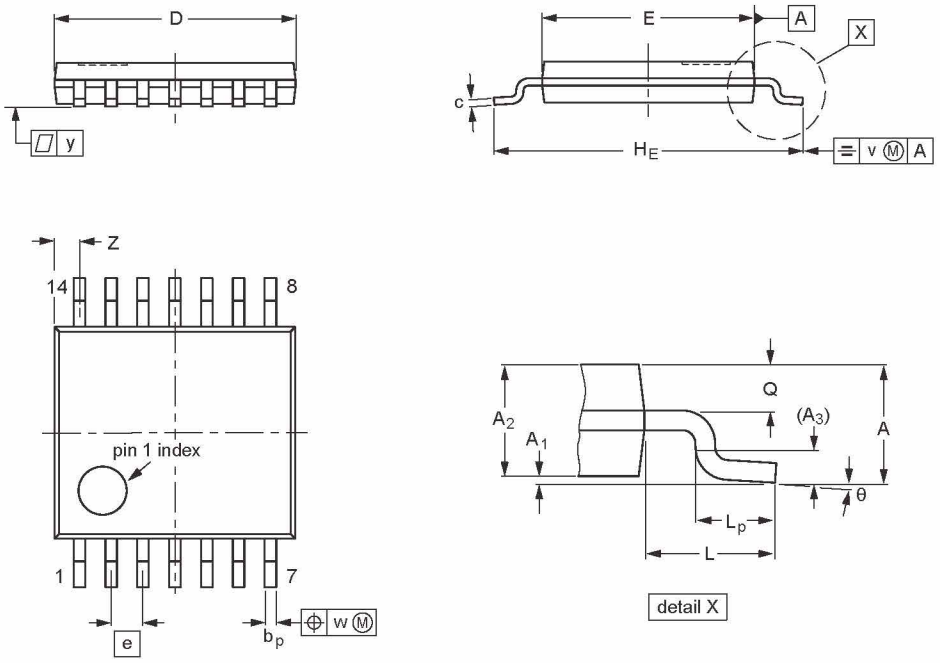
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

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	IEC	JEDEC	JEITA			
TKTSSOP14						05-06-19

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