

Dual 4-Input Positive-AND Gate

DESCRIPTION

The 74HC21 is high-speed Si-gate CMOS device and is pin compatible with pullup resistors with low power Schottky TTL (LSTTL). The device provide the Dual 4-input AND function.

FEATURES

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- TA = -40° to 125° C for all packages

ORDERING INFORMATION

Part Number	Package	Packing	Temperature(TA)	Package Qty
74HC21D	SOIC-14	Reel	-40°C ~ 125°C	2500
74HC21P	TSSOP-14	Reel	-40°C ~ 125°C	2500

PIN ASSIGNMENT

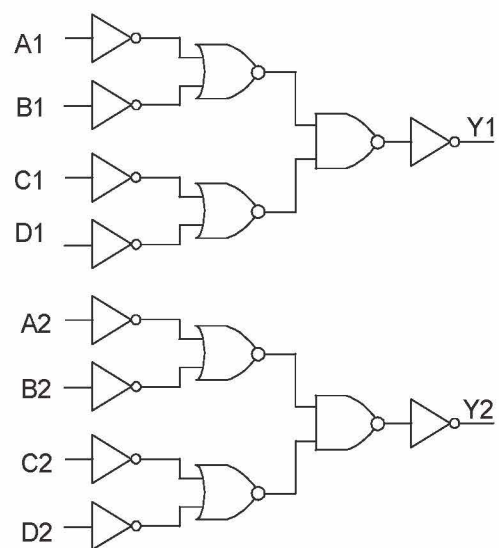
A1	1	14	V _{CC}
B1	2	13	D2
—	3	12	C2
C1	4	11	—
D1	5	10	B2
Y1	6	9	A2
GND	7	8	Y2

FUNCTION TABLE

Inputs				Output
A	B	C	D	Y
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

X = don't care

LOGIC DIAGRAM



PIN 14 = V_{CC} PIN 7 = GND

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-55 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)			
	$V_{CC} = 2.0\text{ V}$	0	1000	ns
	$V_{CC} = 4.5\text{ V}$	0	500	
	$V_{CC} = 6.0\text{ V}$	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low -Level Input Voltage		2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} = -50 μA	2.0 3.0 4.5 6.0	1.92 2.92 4.42 5.92	1.9 2.9 4.4 5.9	1.9 2.9 4.4 5.9	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} = -2.4 mA	3.0	2.48	2.34	2.2	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} = -4 mA	4.5	3.98	3.84	3.7	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} = -5.2 mA	6.0	5.48	5.34	5.2	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} = 50 μA	2.0 3.0 4.5 6.0	0.09 0.09 0.09 0.09	0.1 0.1 0.1 0.1	0.1 0.1 0.1 0.1	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} = 2.4 mA	3.0	0.26	0.33	0.4	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} = 4 mA	4.5	0.26	0.33	0.4	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} = 5.2 mA	6.0	0.26	0.33	0.4	
I _{IL}	Maximum Low-Level Input Leakage Current	V _{IN} = 0 V	6.0	-0.1	-1.0	-1.0	μA
I _{IH}	Maximum High-Level Input Leakage Current	V _{IN} = V _{CC}	6.0	0.1	1.0	1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} =V _{CC} or 0 V	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PHL}, t_{PLH}	Maximum Propagation Delay (Figure 1)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t_{THL}, t_{TLH}	Maximum Output Transition Time (Figure 1)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{IN}	Maximum Input Capacitance	5.0	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Gate)	T _A =25°C, V _{CC} =5.0 V	pF
	Used to determine the no-load dynamic power consumption: P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC}	50	

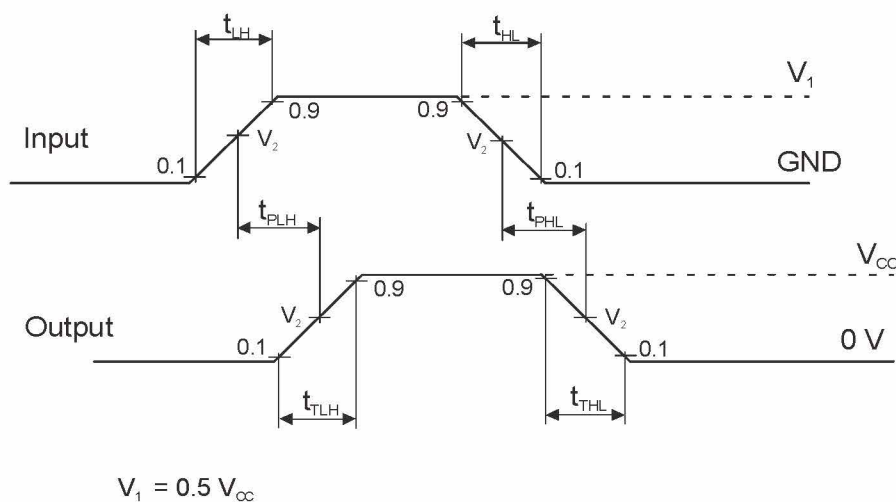
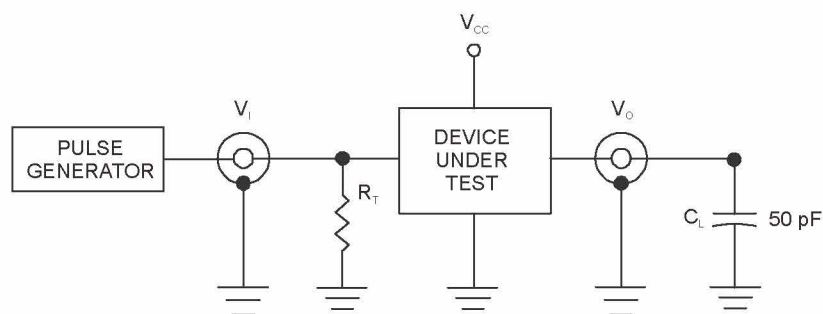


Figure 1. Switching Waveforms

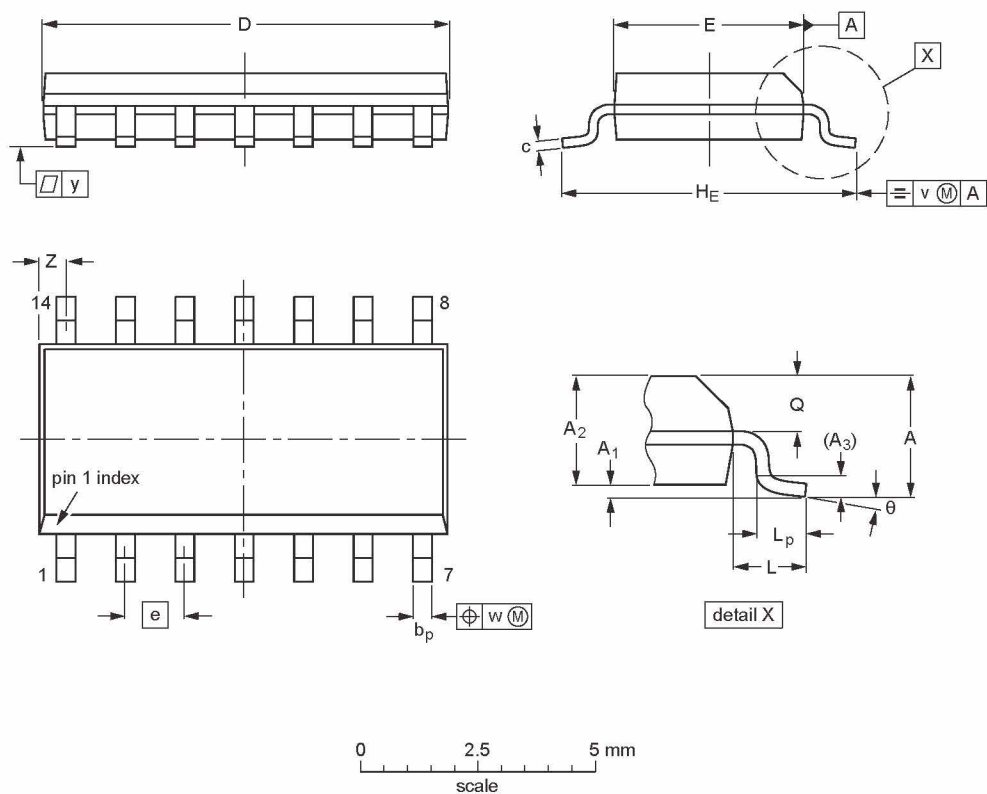


Termination resistance R_T – should be equal to Z_{OUT} of pulse generators

Figure 2. Test Circuit

Package diagram

SOIC14: plastic small outline package; 14 leads; body width 3.9 mm



DIMENSIONS (mm are the original dimensions)

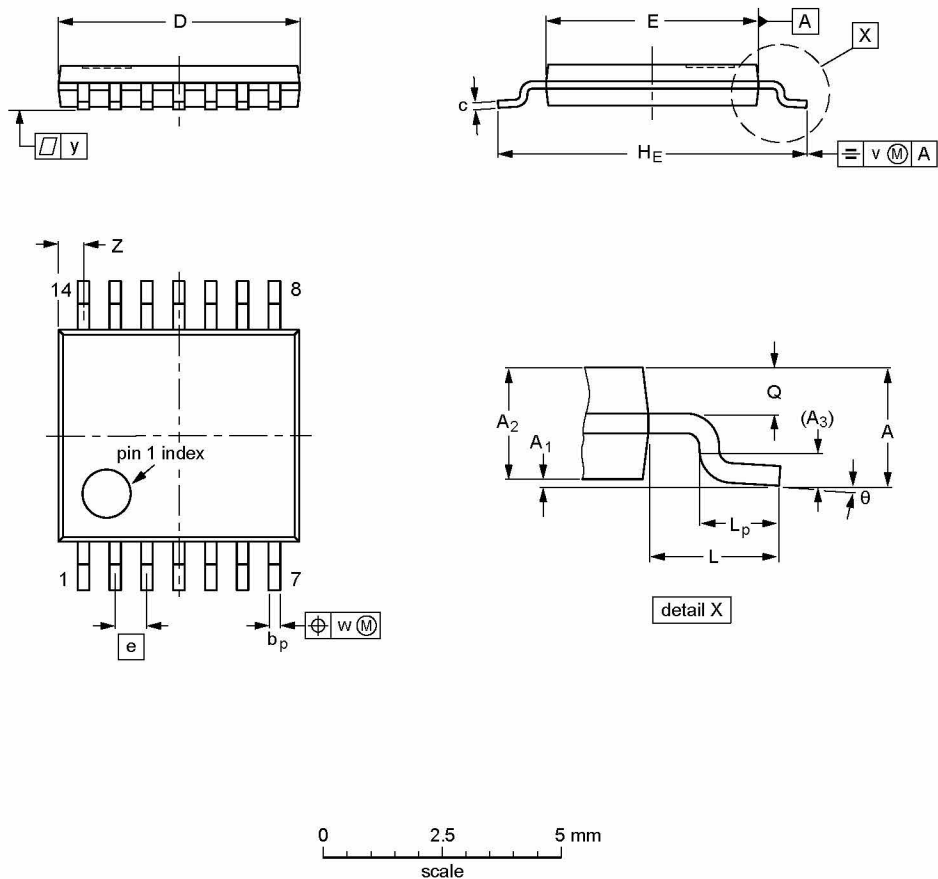
UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TKSOIC14						05-06-19

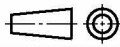
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

- Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TKTSSOP14						05-06-19