

Open-Drain Outputs with hex Inverter

DESCRIPTION

This 74HC05 contains six independent gates, each of which performs the logic INVERT function. The open-drain outputs require external pull-up resistors for proper logical operation. They may be connected to other open-drain outputs to implement active-high wired-AND functions.

The device is identical in pinout to the LS/ALS05. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS TTL outputs.

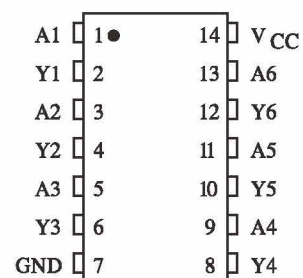
FEATURES

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- $T_A = -40^\circ$ to 125° C for all packages

ORDERING INFORMATION

Part Number	Package	Packing	Temperature(T_A)	Package Qty
74HC05D	SOIC-14	Reel	$-40^\circ\text{C} \sim 125^\circ\text{C}$	2500
74HC05P	TSSOP-14	Reel	$-40^\circ\text{C} \sim 125^\circ\text{C}$	2500

PIN ASSIGNMENT

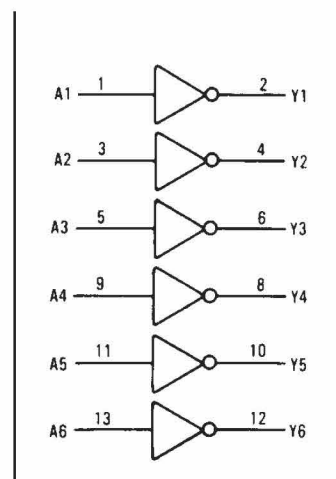


FUNCTION TABLE

Inputs	Output
A	Y
L	Z
H	L

Z = High Impedance

LOGIC DIAGRAM



PIN 14 = V_{CC} PIN 7 = GND

■ MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur.

■ RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 2.0\text{ V}$	0	1000	
	$V_{CC} = 4.5\text{ V}$	0	500	
	$V_{CC} = 6.0\text{ V}$	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

■ DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IL}	Low -Level Input Voltage	V _{OUT} = V _{CC} or 0 V I _{OUT} ≤ ±0.5 μA (T= -55 to 25°C) I _{OUT} ≤ ±5.0 μA (T= 85°C) I _{OUT} ≤ ±10 μA (T= 125°C)	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V _{IH}	High-Level Input Voltage	V _{OUT} ≤ 0.1 V I _{OUT} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{OL}	Low - Level Output Voltage	V _{IN} =V _{IH} I _{OUT} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{IN} =V _{IH} I _{OUT} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
		V _{IN} =V _{IH} I _{OUT} ≤ 5.2 mA	6.0	0.26	0.33	0.40	
I _{IL}	Input Leakage Current	V _{IL} = GND	6.0	-0.1	-1.0	-1.0	μA
I _{IH}	Input Leakage Current	V _{IH} =V _{CC}	6.0	-0.1	-1.0	-1.0	μA
I _{CC}	Quiescent Supply Current (per Package)	V _{IL} =GND V _{IH} =V _{CC} I _{OUT} =0 μA	6.0	1.0	10	40	μA
I _{OZL}	Three-State Leakage Current	V _{IN} = V _{IL} or V _{IH} V _{OUT} = GND	6.0	-0.5	-5.0	-10	μA
I _{OZH}	Three-State Leakage Current	V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC}	6.0	-0.5	-5.0	-10	μA

■ AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
t_{PLZ}, t_{PZL}	Propagation Delay, Input A to Output Y (Figures 1 and 2)	$V_{IL} = \text{GND}$ $V_{IH} = V_{CC}$ $t_{LH} = t_{HL} = 6\text{ ns}$ $C_L = 50\text{ pF}$	2.0	120	150	180	ns
			4.5	24	30	36	
			6.0	20	26	31	
t_{THL}	Output Transition Time, Any Output (Figures 1 and 2)	$V_{IL} = \text{GND}$ $V_{IH} = V_{CC}$ $t_{LH} = t_{HL} = 6\text{ ns}$ $C_L = 50\text{ pF}$	2.0	75	95	110	ns
			4.5	15	19	22	
			6.0	13	16	19	
C_{IN}	Input Capacitance			10	10	10	pF
C_{OUT}	Three-State Output Capacitance (Output in High- Impedance State)			10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate)	Typical @25°C, $V_{CC}=5.0\text{ V}$	pF
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	8.0	

■ Switching Waveform

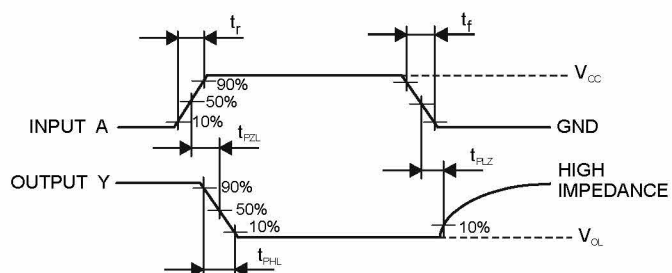


Figure 1. Switching Waveforms

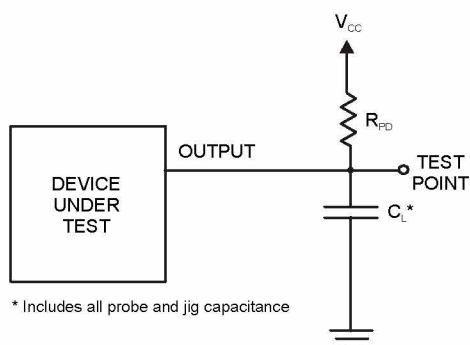


Figure 2. Test Circuit

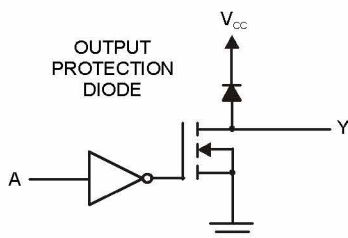
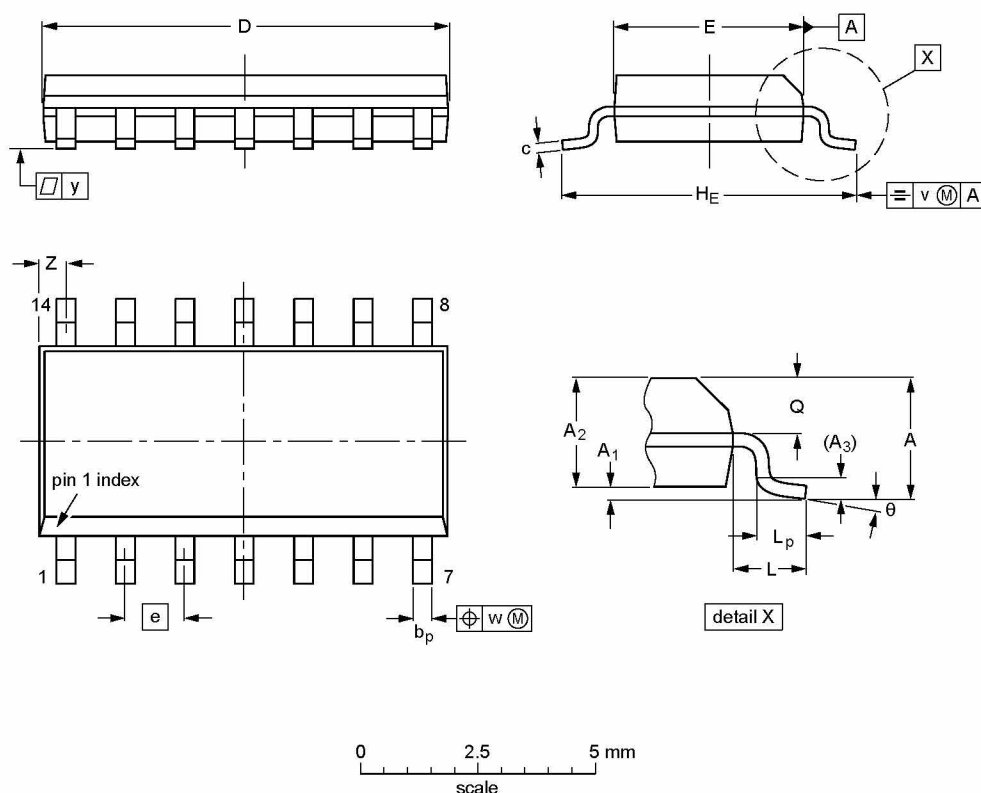


Figure 3. Expanded Logic Diagram (1/6 of the Device)

Package diagram

SOIC14: plastic small outline package; 14 leads; body width 3.9 mm



DIMENSIONS (mm are the original dimensions)

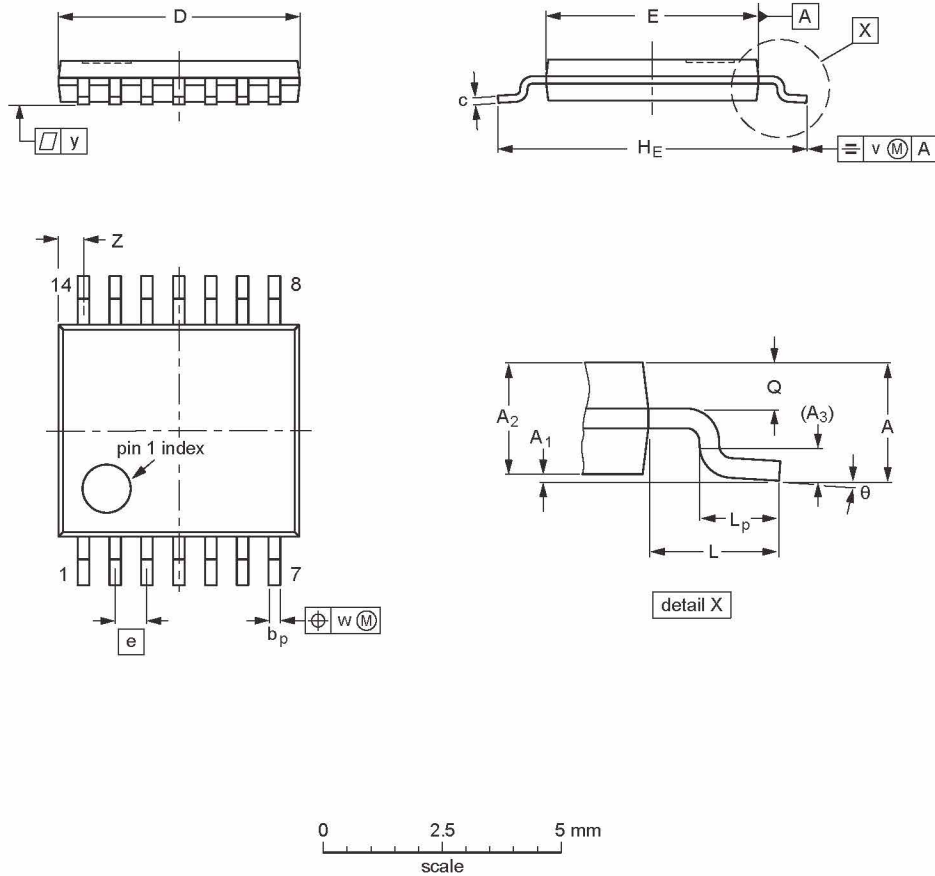
UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TKSOIC14						05-06-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TKTSSOP14						05-06-19